Interconnect Thermal Management of High Power Packaged Electronic Architectures

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Interconnect Thermal Management of High Power Packaged Electronic Architectures

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DEDICATION

To my wife

Megan M. Cook

&

To my parents

Roy and Mary Ann Cook

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The author would like to thank Jesus Christ the Lord and Savior, without whom none of this would have been possible. Next, the author would like to thank Roy and Mary Ann Cook for their encouragement and support over the years. The author would like to thank Dr. Yogendra Joshi and Dr. Ravi Doraiswami for their advice, direction, and serving on the thesis committee for this project. The author would also like to thank Dr. Mostafa Ghiaasiaan for participating in the thesis reading committee. The author also acknowledges financial support for this study from the National Science Foundation and Packaging Research Center at Georgia Institute of Technology. Finally, the author would like to thank the Woodruff School of Mechanical Engineering at Georgia Institute of Technology.

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NOMENCLATURE

Symbols

$\dot{\forall}$	Flow Rate
Q	Heat Dissipation (W)
T_R	Allowable Temperature Rise (K, °C)
R_e	Electrical Resistance (Ω)
I	Electrical Current (Amps)
R	Thermal Resistance (K/W)
L	Material Thickness (m)
A_{cs}	Cross-Sectional Area (m^2)
k	Thermal Conductivity (W/mK)
h	Convective Heat Transfer Coefficient (W/m^2K)
W	Watt
∂	Differential
w	Uncertainty
FR	Instrument Flow Rate
PR	Instrument Pressure Reading
n	Number of Samples
psi	Pounds per square inch
K	Kelvin

Abbreviations

Avg.	Average
BGA	Ball Grid Array
CL	Chip Level
CTE	Coefficient of Thermal Expansion
DAQ	Data Acquisition
FPGA	Field Programmable Gate Array
GPIB	General Purpose Interface Bus
IC	Integrated Circuit
IC (graphs)	Interconnect cooling
NIST	National Institute of Standards and Technology
Pb	Lead
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
Sec	Seconds
SB	Solder Balls
Sn	Tin

Greek Characters

α	Thermal Diffusivity
λ	Separation Constant
ρ	Density
φ	Increment Function
π	pi

γ	Specific Heat Ratio of Air
σ	Unbiased Standard Deviation

SUMMARY

The trend in both the computing and electronic industries is to reduce the size of the electronic components while increasing both their performance and capability. Innovative thermal management schemes are needed in order to reduce the impact of the thermal loads. Most current electronic components are packaged in either a plastic or ceramic container to provide chip and electrical lead protection. Both of these packaging materials have low thermal conductivity, making heat removal from the chip difficult. Thus, heat transfer through the off-chip metal interconnects offers an additional heat removal path, which will enable three-dimensional cooling.

Ball grid array (BGA) interconnects provide an efficient means to connecting packaged high performance chips to printed circuit boards (PCB). As area array bump density increases, reducing Joule heating and electromigration will play an important role in chip and interconnect reliability. Direct cooling of the solder balls is a new approach to removing heat from packaged chips. Jet impingement presents a unique solution for cooling the solder balls. Computational fluid dynamic and heat transfer (CFD/HT) modeling and experiments on plastic ball grid array (PBGA) packages have demonstrated a significant decrease in temperature across the chip, package, and solder balls, when using jet impingement cooling.

The initial modeling showed a 50 K decrease in temperature for a 1 W chip of size 5x5x0.65 mm embedded in a PBGA package of overall dimensions of

17x17x1.16mm. The experiments tested the effectiveness of four different jet hole designs. Each jet hole design had a separate PBGA test chip. Various heat loads were supplied to the chip and solder balls to simulate chip realistic heating conditions. Inconsistencies between each of the PBGA test chips made direct temperature comparisons difficult. Thus, temperature differences between fan cooling from the top and direct interconnect cooling were compared among the four jet hole geometries. The experiments showed that the smaller diameter centered jet hole design was the most effective in cooling both the chip embedded in the PBGA package and also the solder balls.

Finally, a numerical model was created to match the results of one of the experimental jet hole designs. The same properties and boundary conditions were then used in three other models which correspond to the other jet hole geometries. The modeling gave a detailed description of the physics underlying jet impingement cooling of the interconnects. The model predicted that the most effective jet hole design for cooling the chip and solder balls was the centered jet hole pattern.

The experimental results gave insight to the practicality and effectiveness of jet impingement cooling. They were not useful in determining the best jet hole design. The modeling optimized the jet hole design by allowing a direct comparison between each of the impingement cooling designs. Based upon the results from the experiments and modeling, it was concluded that jet impingement cooling of the interconnects is effective for packaged chips.

CHAPTER I

INTRODUCTION AND LITERATURE REVIEW

Cooling Future Electronic Architectures

The consumer is pushing for even higher performance and capability out of the electronic industry. They want a more compact, quiet, aesthetically pleasing computing monster capable of performing several functions simultaneously. Thus, future generation high power electronic architectures will contain multiple high power components for which conventional air cooled heat sinks will be ineffective. An example is system-on-a-package (SOP) technology, which will combine the latest radio frequency (RF), optical, and digital functionalities on a single substrate to create a fast and effective means for computing and communications [Sundaram et al, 2002].

SOP type electronic architectures will be essential to combine video, cell phone, and memory storage devices. Electronic components such as RF power amplifiers, field-programmable gate arrays (FPGA), and microprocessors may collectively dissipate over 100 W of power in such applications in the next few years. Consequentially, to successfully combine multiple functionalities, new ways of integrating thermal management schemes must be studied. Figure I.1 displays the roadmap power dissipation for semiconductor packages [ITRS, 2003].

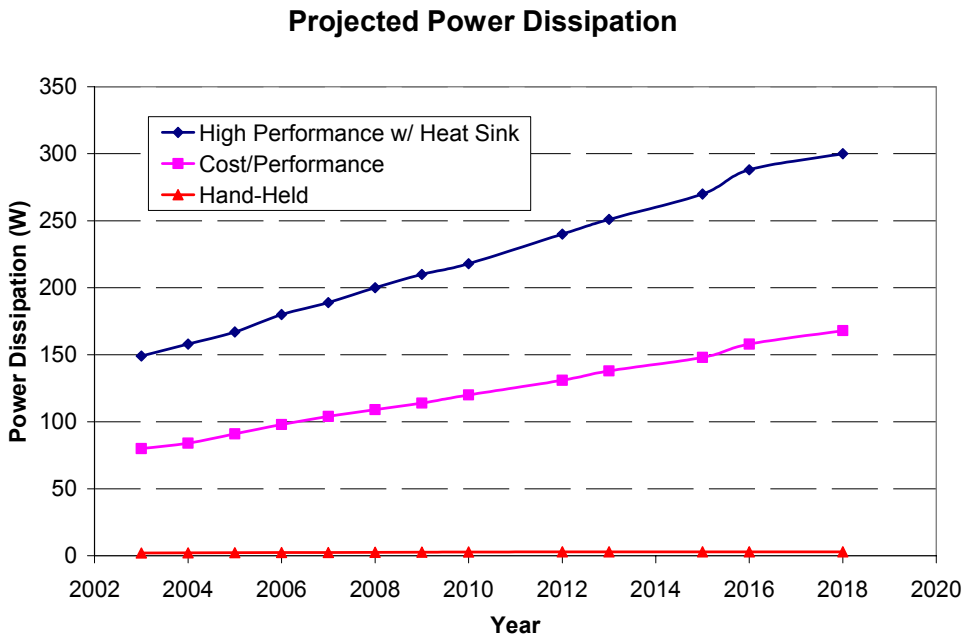


Figure I.1: The International Technology Roadmap of power dissipation for semiconductor packages.

Integrated thermal management devices must be made for a wide variety of applications, ranging from hand-held personal data assistants to large parallel computing structures. Up until recently, electronics have mainly utilized two dimensions; however, three dimensions will be needed for these future architectures. Eventually, integrated circuits (ICs) will be stacked on top of each other, which will be connected to a PCB that will also be stacked on top of another. Conventional thermal management will not work for three dimensional structures, especially if the trends of the electronics industry stay on pace. Figure I.2 shows a general schematic of a three dimensional electronic architecture.

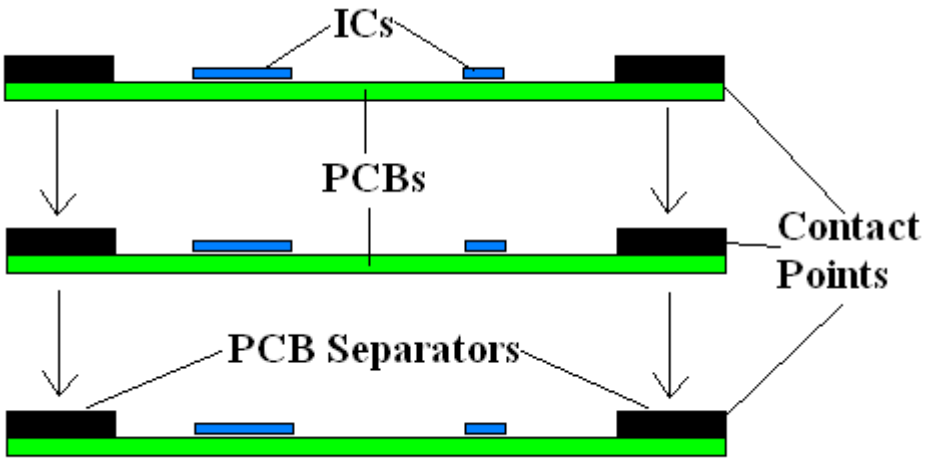


Figure I.2: PCBs are stacked very closely together to conserve space and increase communication between ICs.

Review of Electronic Package Thermal Management

Numerous studies on incorporating thermal management in or on the back of PCBs have been done. This type of cooling is not as effective on packaged ICs, typically due to the high thermal resistance of this path. Also, thermal vias and embedded heat spreaders have been employed to dissipate heat, at a cost of increased complexity of the PCB. These passive cooling methods are effective for today's electronics, but will be insufficient in the future.

Top-level cooling schemes ranging from thermal adhesives and grease to heat sinks and heat pipes are used to dissipate chip level heating. Heat sinks in combination with fans can effectively cool most of today's integrated chips. The amount of heat which can be dissipated is based on the flow rate produced by the fan. The higher the flow rate the better the cooling. The flow rate in m^3/s needed to dissipate a certain amount of heat can be estimated by

$$\dot{\forall} = \frac{0.00083 \cdot Q}{T_R} \qquad \text{(I.1)}$$

where Q (W) is the desired amount of heat to dissipate and T_R (K) is the allowable bulk temperature rise of the coolant [Krinitsin, 2004]. A high flow rate requires a high fan speed which can greatly increase the noise levels. Also, higher fan speeds require are input power, which does not conform to the trend of electronics industry of making more compact devices.

Heat pipes are effective compact cooling devices that utilize vaporization for very high heat removal. Heat pipes are generally made of a good thermally conducting material, such as a copper. The heat is transferred from the source to the working fluid which vaporizes at the evaporator. The vapor travels to the condenser through the core, cools by rejecting heat to the ambient and returns to the heat source by capillary forces created by the wick, which are channels or grooves etched into the bottom of the heat pipe. Heat pipes are often found in the newer laptop computers, in conjunction with a fan because of their compact size.

Some heat pipe reliability issues are leakage and dry out. Over time, cracks may develop due to thermal cycling and the fluid may leak out which would render the heat pipe useless. Dry out occurs when the entire supply of liquid coolant is depleted. This also renders the heat pipe essentially useless. Heat pipes are very effective in removing heat from high performance chips, but still have some reliability issues and are limited to a specific power range due to dry out limits.

Direct cooling of the off-chip metal interconnects is a new approach to removing heat from packaged high performance ICs. This technique could be used in conjunction with top surface mounted thermal management devices to augment heat removal. The

interconnects leave a small gap between the packaged chip and PCB, which can be utilized for incorporating a thermal management scheme. Since this space is very limited, fans and conventional heat sinks are not practical solutions. Jet impingement presents a unique solution for cooling solder balls. Cambell et al. [1998] have shown that micro jets can effectively cool the top surface of laptop computer processors, while requiring very little space. They can also be used to cool the solder balls and bottom of the chip.

This research is mainly focused on ball grid array (BGA) type packages, although the same thermal management scheme could be implemented with other area array packaging architectures. BGA type packages are used to house a wide variety of microelectronics ranging from microprocessors to field programmable gate arrays (FPGA). They are used with these high performance ICs because of the improved electrical performance from the array of very short, low inductance solder balls [Joiner et al., 2002].

BGA packaged chips can be cooled using several methods. Kromann et al. [1996] discusses two solutions for chip level cooling. The first is to attach a heat sink or spreader to the top surface of the package and blow air across it. The second is changing the package casing to a more thermally conductive material. While this may address chip level heating, it does not aid in removing the Joule heating generated in the solder balls.

Jet impingement offers a unique cooling strategy for rejecting heat in the solder ball interconnects. Both air and liquids can be used as the heat transfer medium. Air is convenient to implement because it involves less components and assembly when compared to a liquid. Liquid cooling may be necessary to handle future higher power,

higher heat dissipating electronics. Interconnect cooling using air jets is studied extensively through numerical modeling and experimentation in the following chapters.

Off-Chip Metal Interconnects

Today, wire bonding is the dominant method for attaching electronic chips to PCBs because it provides a flexible, reliable, and robust connection. Key drawbacks of wire bonding include input/outputs (I/Os) limited to the perimeter of the chip, long lead lengths, and limited heat removal paths [Adams et al, 2000]. As chips require more input/output (I/O) connections, the wire diameter decreases, which reduces the electrical reliability of the wire lead. Probably, most of the future's high performance ICs will utilize an alternative interconnect method.

An innovative attachment technology in the microprocessors and packaged IC industry became popular in the 1990s called flip chip [Adams et al, 2000]. Flip chip involves connecting a bare silicon die to a PCB directly using solder joint arrays and underfill material. Since the chip is bare, a thermal management scheme can easily be implemented above it. However, this may not be sufficient to cool the solder joints. A solder joint can take on many different geometries, but the most common is the ball. The solder ball interconnect significantly reduces the lead length, which decreases the electrical resistance compared to a wire bond. Also, I/Os can be placed across the entire face of the IC, which allows for the development of significantly more complicated IC architectures. The underfill is used to reduce the coefficient of thermal expansion (CTE) mismatch between the solder joint and IC, however it is usually a poor thermal conductor

typically around 1 W/mK. Flip chip technology has several reliability concerns. First, as the solder ball size decreases with the increase of I/Os; CTE mismatch, electromigration, and thermomigration become a significant problem. Second, the IC has no protective casing, which limits its applications to non-harsh environments.

Most chips are packaged in ceramic or plastic containers to address some of the reliability issues present in both wire bonding and flip chip technologies. Both of these packaging materials have low thermal conductivity, making heat removal from the chip difficult. While adding a cooling scheme to the top surface of the package can reduce the chip level thermal loads, the metal electrical leads and thermal vias in direct contact with the chip offer an additional heat removal path.

Some electronic packages have heat spreaders embedded in them to aid in removing heat from the chip. The spreaders are usually located directly on top of the chip. This helps bring the heat generated in chip to the surface of the package. Then some type of top level thermal management device removes the heat from the embedded spreader. These embedded spreaders are limited to chips which utilize flip chip connection within the package, and only remove chip level heating. Figure I.3 shows a packaged chip with an embedded copper spreader and thermal vias.

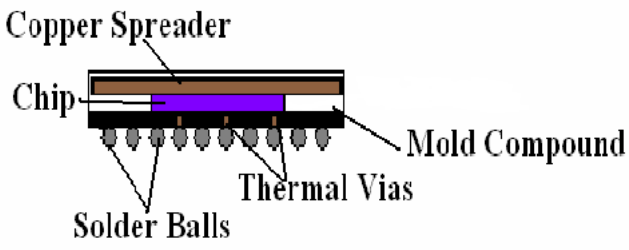


Figure I.3: A packaged chip with an embedded copper spreader and thermal vias to alleviate some the heat generated in the chip.

BGA interconnects provide an efficient means to connecting packaged high performance chips to PCBs. As the area array solder ball density increases, Joule heating will play an important role in chip and interconnect reliability. Future interconnect reliability issues which are not necessarily a problem today are quickly developing into an area of concern. In order to achieve higher performance and functionality more I/Os will be required, which leads to reducing both the diameter and pitch of the solder balls. The solder ball's diameter are approaching a couple of tens of micrometers [ITRS, 2003]. Micro voids and cracks, which are inherent in the reflow process and can also occur during Joule heating, on the order of magnitude of the solder ball diameter will have a greater affect on the mechanical and electrical reliability of the integrated circuit. Figure I.4 shows the roadmap for pad pitch lengths for full grid array packaged ICs for the next 12 years [ITRS, 2003].

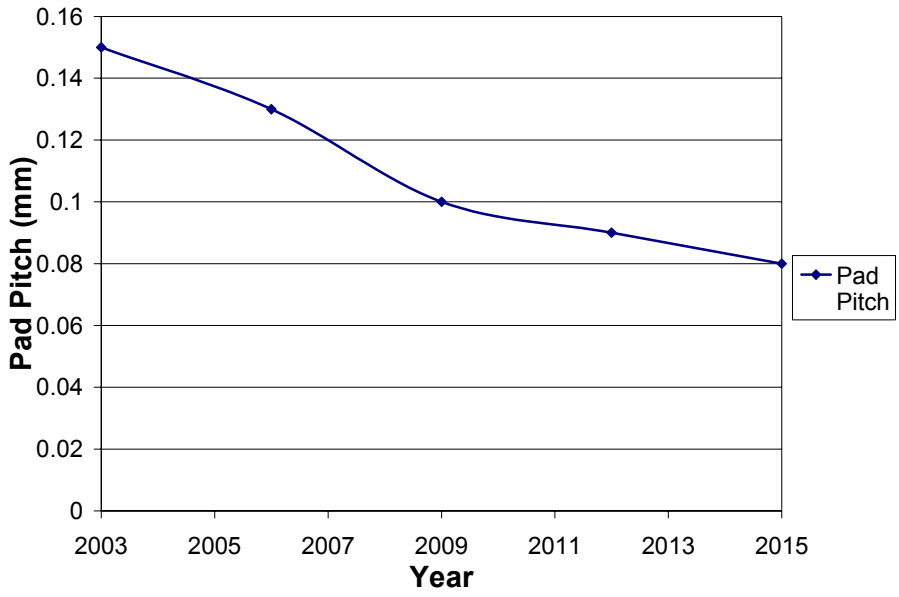


Figure I.4: The projected Pad Pitch for full grid array packaged integrated circuits.

Joule heating, in addition to chip level heating can significantly reduce the clock speed and I/O rates, while increasing noise and leakage power [Campbell et al, 4]. Also, as solder balls decrease in size, reliability issues such as coefficient of thermal expansion (CTE) mismatch, thermomigration, and electromigration become more of a problem as seen with flip chip technology. Ye et al [2003] have shown that current stressing caused by electromigration significantly contributes to Joule heating in solder balls. Solder joint interconnects are the most significant bottleneck for electrical and mechanical reliability issues for microelectronics [Cartwright, 2003].

In addition to joule heating, three other heat generating sources contribute to interconnect heating. Chip level heating caused by transistor switching can greatly increase the temperatures in the interconnects. The chip has a direct metal link to the solder balls through electrical leads and thermal vias so a significant amount of heat transfers to the interconnects. The second is heat generated in the PCB. The ground plane and power leads generate heat due to current passing through them to supply power to the packaged chip. The third source of heating is due to the environment around the package. Under certain conditions, such as environmental testing, heat transfer could occur due to the elevated external temperature. Joule, chip, environmental, and PCB heat generation all contribute to interconnect heating, which can cause several reliability issues.

Coeffiecient of Thermal Mismatch, Electromigration, and Thermomigration

Integrated circuits require external power in order to perform their functions. Power is supplied through the off-chip metal interconnects of the IC. In the case of the BGA the power is supplied through the solder balls. Joule heating is created due to a current and electrical resistance interaction within the solder balls. The equation used to obtain the rate of heat generated in Watts is given by

$$Q = I^2 \cdot R_e \qquad \text{(I.2)}$$

where I is the current (Amps) flowing through the solder ball and R_e (Ohms) is the electrical resistance. As the solder ball's volume decreases, the resistance increases, which leads to internal heat generation. It may also lead to coefficient of thermal expansion (CTE) mismatch driven stresses and thermomigration, which may cause complete dislocation of the solder ball from either the bond pad on the PCB or the metal layer on the packaged chip, which would result in an electrical failure.

CTE mismatch causes two dissimilar metals, in contact with each other, to expand at different rates upon heating. This applies a large amount of stress between the solder joints and metal bond pads. Flip chip type technology utilizes an underfill to help alleviate some of the stresses involved in this problem. Underfills are generally made up of a composite epoxy matrix with ceramic fragments [Qu et al., 1997]. As the gap between the PCB and IC decreases, underfill will become more difficult to apply. One of the primary failures in underfilled packages is delamination, which involves the separation of the underfill with either the PCB or chip [Patwardhan, 2002]. Also,

underfills are generally not good thermal conductors, which may create other reliability issues with electromigration and thermomigration.

Packaged ICs are generally not underfilled due to their larger pitches and ball sizes, however as their pitch and solder ball diameters decrease CTE mismatch will be a major concern. This reliability concern leads to higher temperatures in both the solder balls and the package. Steps have been taken to reduce CTE mismatch by changing the type of metals used for both the solder balls and package bonding pads. Some packaged architectures are underfilled to alleviate CTE mismatch, but they are still susceptible to the same reliability issues with flip chip technology. These enhancement techniques have increased the reliability of both packaged and flip-chip technologies; however, with future chips requiring more power, reducing the interconnect temperature directly may also be required.

Electromigration is caused when large current densities produce a mechanical force on the atoms, which causes them to move in the direction of the current. Micro cracks and voids develop near the cathode side while hillocks form on the anode side. This indicates electromigration forces material to shift from the cathode toward the anode side of the interconnect [Ye et al, 7]. The most common current density found in the literature at which electromigration has been shown to occur is around 10^4 A/cm^2. However, electromigration has been shown to occur under much lower current densities, depending on operating environment and quality of the off-chip metal interconnects. High current density can occur when the solder ball is very small or when there are large voids in it, resulting in bottlenecks to the current flow. Elevated temperatures have also been shown to induce electromigration at much lower current densities. Possibly

reducing the Joule heating induced temperature rise in the solder balls can reduce the reliability concern of electromigration. Figure I.5 illustrates the effects of electromigration in a solder ball interconnect [Ye et al, 2003]

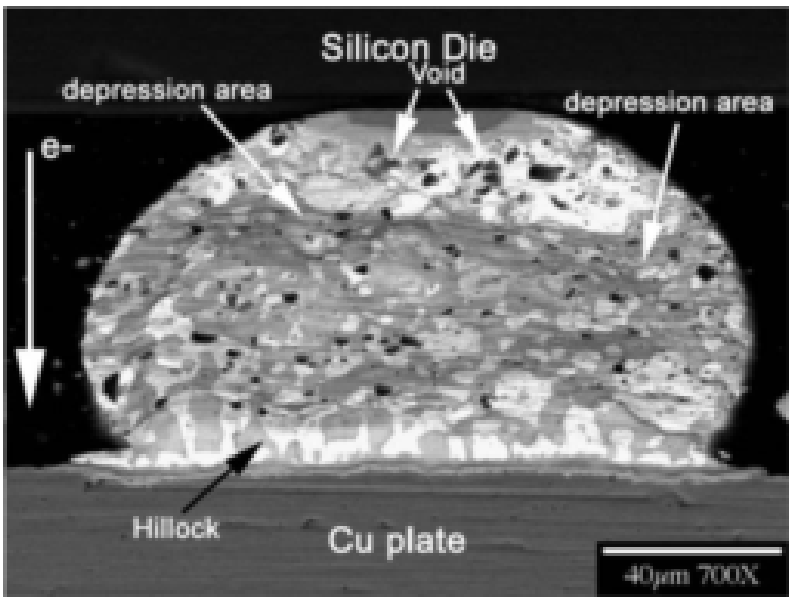


Figure I.5: Micro-cracks and hillocks as a result of electromigration in a solder ball interconnect.

Thermomigration was discovered when conducting experiments electromigration [Ye et al, 2003]. The experiment involved a silicon chip mounted with two solder balls that were connected together with an aluminum trace. The chip was underfilled and bonded to a FR4 PCB with copper traces to supply power. High current was passed through the solder balls and aluminum trace for several hours. The silicon die was then observed under a scanning electron microscope and evidence of thermomigration had been found. Voids and microcracks were formed on the anode side of the trace, which is

the opposite effect of electromigration. This experiment showed evidence of thermomigration having a greater effect then electromigration in some cases.

Thermomigration is present when large thermal gradients exist in the solder ball interconnects. These gradients cause the atoms to move from a hot area to a cooler area, which creates micro cracks and voids [Ye et al, 7]. These voids can reduce both the mechanical and electrical reliability of the ball. Joule heating may be reduced by cooling the off-chip metal interconnects, which will decrease temperature gradients throughout the electronic package.

Signal Quality Degradation

BGA type packaging has greatly reduced the effect of both the capacitance and inductance in the solder ball interconnects because of their shorter lead length. Capacitance and inductance can cause a reduction in the velocity of signal propagation, which can reduce the performance of the IC [Chien, 1995]. These problems are generally seen in packaging that utilize wire bonding techniques with long interconnect lengths. Capacitance is a material's ability to store a charge. As the length of the interconnect increases its capacitance also increases, which can slow the electrical performance of the IC. Inductance is a material's ability to oppose any change in current through it. Inductance is a function of the length of the material, thus the shorter the interconnect length, the lower the inductance. Based on the definition of inductance and capacitance they can also be directly related to the electrical resistance of a material which is strongly dependant on temperature.

Interconnect electrical resistance is a major concern for ICs today. An increase in the electrical resistance of the solder ball interconnect can greatly reduce the performance of an IC. As more Joule and chip level heat is generated, the resistance of the electrical leads further increases. Many of the previously discussed reliability concerns stem from an increase in resistance. This heating can create micro voids and cracks which can induce electromigration and thermomigration. CTE mismatch also has a direct relation to an increase in resistance. Reducing the resistance increase by Joule heating in the interconnects will help alleviate these reliability concerns.

Beyond the mechanical and electrical reliability issues lay a large number of signal quality problems. Both chip level and off-chip metal interconnect heating can greatly reduce the capability of an IC. The heat generated increases the resistance in the solder balls which can lead to power leakage and electrical noise.

Power leakage is a direct result of leakage current. Leakage current is the current that flows from the protective ground to the earth ground [Condor, 2004]. It is often found to occur in the transistors of the IC but has also been seen in high current flow through off-chip metal interconnects. Leakage current can be extremely sensitive to temperature. It increases exponentially with an increase in temperature [Transmeta, 2002]. Reducing the temperature of the interconnects will decrease leakage power problems.

There are two types of electrical noise. The first is called thermal or Johnson noise and is due to lattice vibrations in a material caused by heat. The second is shot noise which results from electron flow through an electric field [Ritter, 2004]. Both

types of electrical noise can be reduced but can not be completely eliminated. Any noise beyond the inherent noise can impact the reliability.

It has been shown in a study by Jones [Jones, 2002] that excess electrical noise is a sensitive indicator of quality and reliability in ICs. The quality of an electrical device depends on the number of defects in the materials during its fabrication. It also depends on the quality of assembly of a particular electronic architecture. Some of these variables can be controlled through finer processing, but some are inevitable. The quality of the device manufacturing can affect its reliability. The excess noise may be caused by parasitic resistance, loss in a capacitor, a leakage current or defect in the material [Jones, 2002]. This excess noise can be measured to predict the life time of the IC. Cooling the interconnects and IC decrease the excess electric noise.

Thermal Management of Packaged Integrated Circuits

As seen above spatial and temporal temperature gradients near an integrated circuit impacts mechanical, electrical, and chemical effects in packaging reliability. Thermal management schemes have been implemented on top of the package or in the PCB to reject the chip level heating. In addition to external thermal management devices, copper spreaders and thermal vias have been embedded into electronic packaging to transport heat from the integrated circuits. These thermal management schemes do not directly address the problem of Joule heating in the off-chip metal interconnects. Thermal management addressing the cooling of the interconnects is crucial to increase the reliability and operating life time of the integrated circuit.

It has been shown in a numerical study of a molded array plastic ball grid array (MAP PBGA) conducted by Adams et al. [Adams et al, 2000] that most heat dissipated from the chip without any thermal management is through the bottom of the package through the laminate substrate and solder balls. Two other cases were studied and the results are in the figures I.6 and I.7 [Adam et al, 2000]. Figure I.6 illustrates the possible heat paths from the junction of the chip. Figure I.7 shows the results of the analysis with no thermal management, a 4-layer laminate substrate, and copper heat sink attached on top of the package.

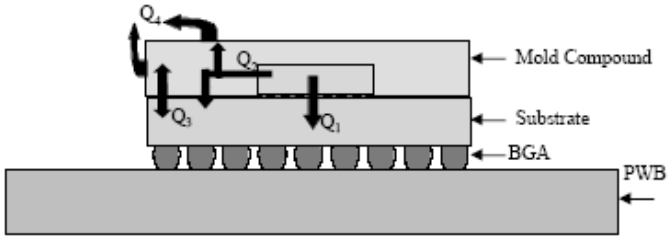


Figure I.6: The possible heat paths through a MAP PBGA package.

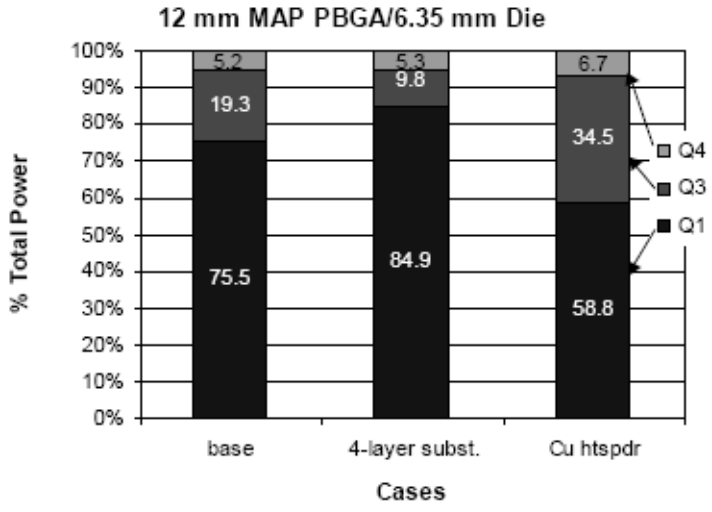


Figure I.7: Total power percentage of dissipation paths for various thermal management schemes in the MAP PBGA.

Figure I.7 indicates that most of the heat dissipated from the IC travels through the bottom of the package. Q1 represents the percentage of heat generated that is transferred from the IC to the bottom of the package. Q2 represents the percentage of heat that travels through the mold compound, which travels out both the top and bottom surface of the package. Q3 represents the percentage of heat dissipated from the top surface of the package. Even with a top level copper heat sink, a majority of the heat travels through the bottom of the package.

Jet Impingement Cooling

The idea of jet impingement has been around almost since the IC was created. It has been studied in very great detail over the years because of its high heat transfer rates which can be achieved in the stagnation region of the flow [Guarino et al., 2001]. The jets can also be arranged in any fashion to suite the geometry and large thermal gradient areas of electronic architectures. Jet impingement has been shown to be effective in cooling laptop computers. In a study by Guaruno et al. [2001], jet impingement was simulated in a laptop computer to test its effectiveness. The study examined the effects of adding an impinging jet to a heat pipe cooled microprocessor. The simulation was run with jet impingement, heat pipe cooling, and finally with both jet impingement and heat pipe cooling. The results showed a significant decrease in temperature when just using the jets, while a much greater improvement when the heat pipe and jet were used in combination.

In 1989 William Hamburgen [Hamburgen, 1989] devised and patented a method for cooling packaged electronic components by using an array of nozzles fabricated in the circuit board. The backside of the circuit board contained a chamber, which held a greater pressure then ambient. This pressure difference forced air through the nozzles and would blow on the under side of the packaged electronic component. The electronic packages around 1989 were mainly pin and wire type packages. The interconnects were rather large and as a result Joule heating had little impact on them. Hamburgen's idea was another method for cooling the IC in packaged electronics and did not directly address cooling the off-chip metal interconnects.

Several factors were looked at in considering jet impingement for cooling the off-chip metal interconnects of packaged ICs. The first consideration was addressing the impact of putting several additional holes in the power and ground planes of the PCB. The ground and power planes are generally large masses of metal embedded into the PCB. Adding these additional holes in these planes may contribute to additional Joule heating by adding additional impedance to the planes.

Generally, if a PCB is going to be used to supply power to high performance ICs, then the ground and power planes are designed to handle high current flow. The addition of micro-sized holes will not change the area of the ground plane significantly enough to cause any additional joule heating. For example, a small ½ ounce ground plane is approximately 0.017 mm in thickness and it is assumed to be 17 x 17 mm in cross-section. The resistance of this ground plane without the jet holes is around 1.01×10^{-9} ohms. If 50 jet holes with a diameter of 0.350 mm are incorporated into the ground plane the resistance becomes 1.03×10^{-9} ohms. The addition of the jet holes caused a 1.7 %

increase in resistance. The jet hole diameter used in this example was rather large when compared with the pad-pitches for future package ICs. Jet holes will have less significance on ground and power plane impedance as their diameters decrease with the trends of the electronics industry.

The second consideration was the electrical noise effects with the addition of holes in the ground and power planes. Current is the main cause of electrical noise between the two planes. This generally occurs when the two planes are close together or there are a large number of plated vias that intersect both planes. Since, the jet holes are not plated the additional vias will not increase the noise between the planes.

The third consideration was the jet holes may affect the circuitry in PCB. Thus most of the jet holes must be implemented toward the center of the package IC for both periphery array and full grid array type architectures. The electrical leads in the PCB generally utilize the first several rows of the peripheral solder balls for I/Os. The PCB is very complex around the peripheral interconnects due to the electrical inductors, transducers, and electrical leads needed to communicate with the IC. The central solder balls are mainly used for power and ground connects, which require simple circuitry in the PCB. Figure I.8 shows a plastic ball grid array packaged Xilinx field programmable gate array chip's solder ball layout.

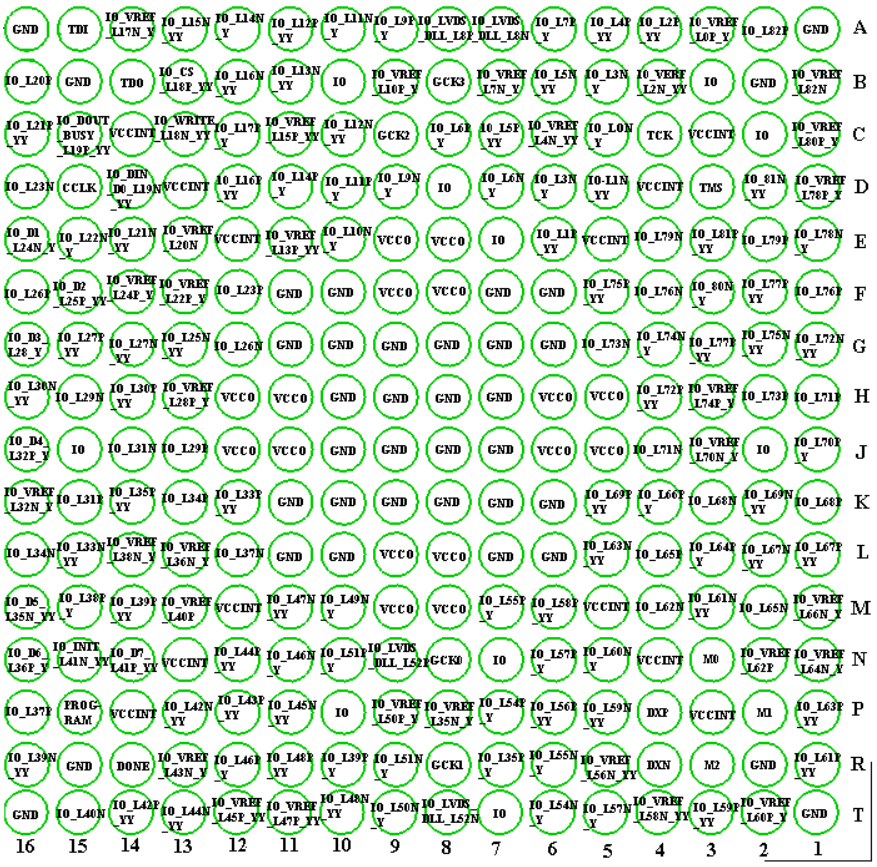


Figure I.8: Solder ball I/O, power, and ground interconnect layout of a Xilinx PBGA packaged FPGA.

Off-chip metal interconnect cooling in addition to chip level and packaging thermal management schemes make 3-D heat dissipation possible. Implementing a package level cooling scheme or even a top level heat sink in addition to a direct interconnect cooling scheme will maximize heat dissipation. The IC dissipates the most heat so reducing the thermal resistance of the package in both the planar and vertical directions will reduce the maximum operating temperature. It will also increase both the mechanical and electrical reliability of all the components which comprise a typical packaged IC.

Three-dimensional Electronic Architectures

A large bottleneck in the design and development of high performance digital systems has been transmission delay between logic circuitry. This delay is mainly due to the distance between IC components on planar electronic architectures. As electronics become more powerful, the need for three-dimensional stacking of multiple PCB and ICs will be essential for conserving space. Three dimensional electronic architectures reduce the distance between the ICs, which reduces transmission delays [George et al., 1995]. They are also seen in servers, parallel processing centers, and many other electronic systems. A major concern for these systems is effectively cooling the ICs, which are densely packaged together in three-dimensional structures.

Generally these types of systems are cooled by fans distributed through out the stacked layers of electronics. The same hot air circulates through the fan and cools the ICs. Jet impingement cooling from the PCB may greatly aid in cooling these 3-D structures. The layers of PCBs could have jet holes underneath the ICs which could reduce the interconnect and chip temperatures. A single compressor or pump could supply several layers of ICs with either air or a cooling liquid. Another advantage of using a compressor type system is that it can draw cool air from another location outside of the casing of the stacked electronics. There are many possible uses for direct interconnect cooling for different electronic architectures.

CHAPTER II

INITIAL NUMERICAL MODELING OF DIRECT INTERCONNECT COOLING ON A PLASTIC BALL GRID ARRAY PACKAGE

The initial finite element thermal and fluidic modeling was used to obtain an idea of how effective jet impingement cooling could be on packaged ICs. Electromigration, thermomigration, and CTE mismatch are not modeled below, due to the complexity of these phenomena. An estimation of the Joule heating caused by these factors will be addressed within the model. If heat generated throughout the package and solder balls can be reduced with direct cooling of the solder balls then the impact of these reliability issues will be less. The initial modeling described below is detailed in a paper by Cook et al [Cook et al, 2004].

Initial Modeling of a Plastic Ball Grid Array Die

ICs, microprocessors, FPGAs, and a multitude of other electronic chips are packaged in many different materials and geometries. A variety of packages are centered on the idea of wire bonding and only use metallic pins on the periphery of the device to connect with a PCB. Some packages are also designed to mimic the flip chip method.

BGAs contain an array of solder balls either on the perimeter or across the entire surface of the package and are used to connect with the PCB. Inside the package the chips are either wire bonded or flip chipped to leads that carry the I/O to the outer interconnects. Electronic chip packages often incorporate thermal spreaders and vias to dissipate the heat produced by the IC. The thermal spreaders transfer the heat to the top surface of the package so that it can be removed through another spreader to flowing air. Thermal vias transfer heat to the packages' interconnects which is then removed by a thermal spreader embedded into the PCB. Vias can also be used to transfer heat to the outside layers of the package. The package level thermal vias reject heat from the IC, but are not as effective for the interconnects. A model that incorporated these intricate details of the electronic package was necessary in order to see how heat moves through packages.

A commonly used package to house high performance chips is the plastic ball grid array (PBGA). The encased chip is wire bonded to a laminate substrate, which contains all of the electrical leads and thermal vias that connect to solder balls on the bottom of the package. The laminate substrate is basically a small PCB, which is made up of several copper layers and electrically insulating material such as FR4 or low temperature co-fired ceramic (LTCC). The plastic molding encapsulates the IC to hold it and the wire bonds in place.

The experiments were run with a PBGA dummy package with dimensions of 17x17x1.16 mm. Thus, the modeling was based on this geometry. The PBGA model did not include the solder mask layer and bonding wire. These components were excluded because they do not conduct a significant amount of heat away from the chip and would significantly increase the complexity of the model. The mold compound, silicon chip,

chip-attach material, laminate substrate, thermal vias, and solder balls were included in the model. The package was connected through 256 63Sn/37Pb solder balls to a 4 layer PCB. Table II.1 lists the properties and heat loads used in the PBGA model. Only $1/8^{th}$ of the package and PCB was modeled due to symmetry and also to reduce computational time.

Table II.1: A list of the material properties used in the PBGA model.

Properties & Heat Gen.	k (W/m K)	C_p (J/kg K)	ρ (kg/m^3)	Q (W)
Silicon Die	117.5-0.42(T-100)	712	1685	1.5
Solder Balls	40.9	150	8340	3.4x10-05
Laminate Substrate	1.1	547	2000	NA
Thermal Vias (copper)	401	385	8933	NA
Chip Attach Material	2	500	3500	NA
PCB	1.1	289	1978	NA

ANSYS and Fluent were used to model both the thermal and fluid dynamics aspects of the system described above. Fluent was used to model the air path from the outlet of the compressor to the bottom side of the PBGA package. Sixty-four round jets were assumed incorporated into the PCB. The inner dimensions of the pressure chamber, mounted on the backside of the PCB, were 17x17x10 mm. The tube connecting the pressure chamber and compressor had a length of 40 mm and a diameter of 15 mm. The jets were 0.6 mm in height and 0.5 mm in diameter. The distance between the PBGA

package and the PCB was 0.6 mm. The air velocity and heat transfer coefficients were found using Fluent and used as boundary conditions in ANSYS. ANSYS was used to model the conductive heat transfer through the PBGA package.

Two conduction models were created of the PBGA package. The first was a baseline model using only ANSYS, which consisted of estimated boundary conditions based on natural convection between the chip and PCB and forced convection on the top surface of the PBGA. The second model involved Fluent for calculating the fluid velocity and *h* when jet impingement cooling was implemented. Once the heat transfer boundary conditions were found in Fluent they were applied to the conduction model of the PBGA in ANSYS.

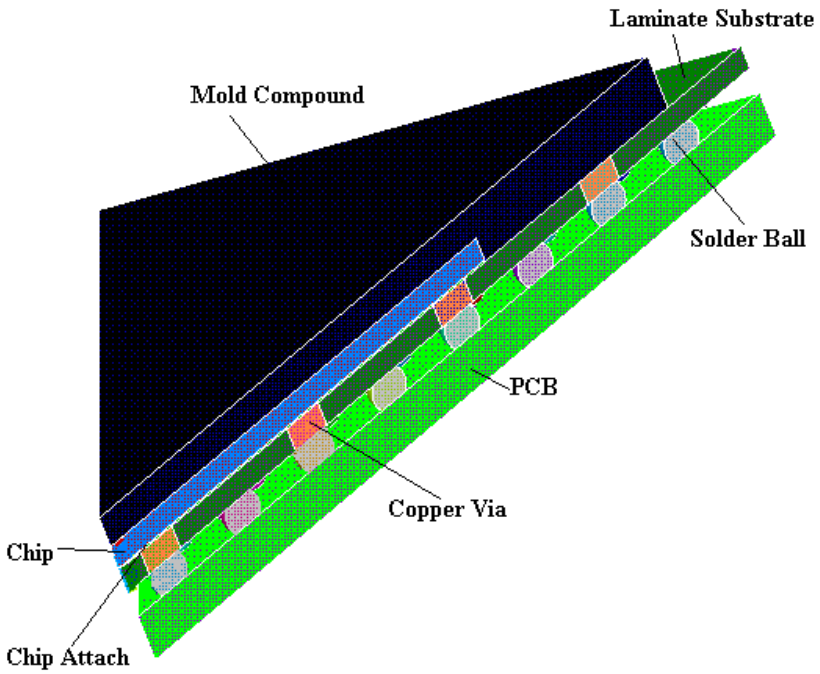


Figure II.1: The 1/8th simplified PBGA layout for modeling consisting of; copper vias, 63Sn/37Pb solder balls, chip attach material, silicon chip, mold compound material, and PCB.

Baseline Plastic Ball Grid Array Model

Both the solder balls and chip were given volumetric heat loads to simulate the Joule and chip level heating respectively. A volumetric heat load of 11,593 W/m^3 was specified for the solder balls and $2.7x10^7$ W/m^3 (a total of 1.5 W) was specified for the chip. These heat loads were based on the thermal loads illustrated in table II.1 and the volume of the solder balls and chip. For the interconnects the heat loads were estimated by assuming a current of 400 mA. The top of both the mold compound and laminate substrate were given an *h* of 30 W/m^2K to simulate cooling produced by a fan. The sides of the mold compound and laminate substrate were given an *h* of 25 W/m^2K to simulate indirect cooling from the fan. An *h* of 5 W/m^2K was specified for the backside of the PCB. The sides of symmetry were given adiabatic boundary conditions. An *h* of 3 W/m^2K was specified for the solder balls and underside of the chip to simulate natural convection. These boundary conditions were not based on direct analytical calculations but on typical ranges for low flow air cooling and natural convection [Incopera et al, 2002]. The model was solved as steady state in ANSYS. Several models with identical boundary conditions were run with increasingly finer grids to obtain a temperature difference within 0.05 K between the various grid sizes. This was done to achieve grid size independent results from the model.

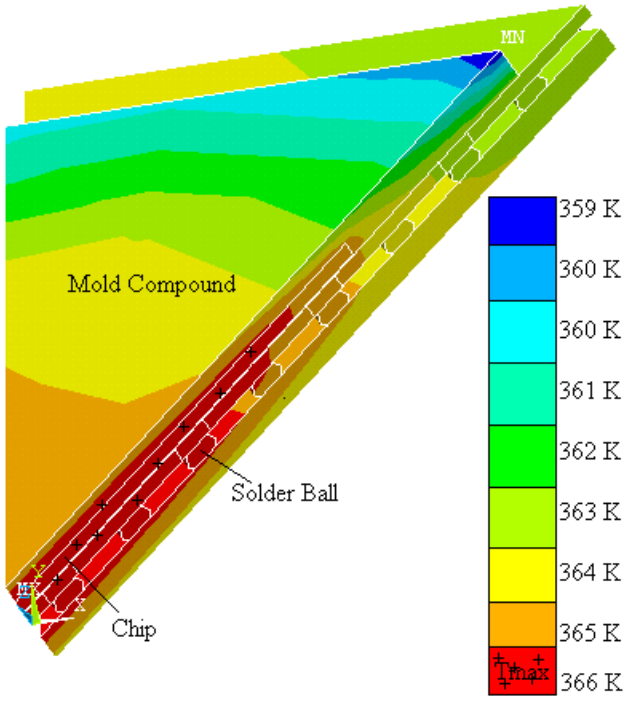


Figure II.2: The PBGA package baseline model which has no thermal management.

The chip center was around 366 K, which represents the maximum temperature from the entire domain. The chip temperature gradually decreased to 365 K toward the periphery. The mold compound encasing the chip conducted heat poorly due to its low thermal conductivity. The solder ball temperature ranged from 362 K to 365 K. Heat was transferred from the chip through the copper vias to the solder balls, which contributed to their heating. The left corner of the mold compound was the coolest with a temperature of 359 K. This occurred because of the external top and side surfaces from which heat can be removed through forced convection. The temperature of the PCB was relatively uniform ranging from 362 K to 363 K. Overall, the largest temperature gradient throughout the package was 6 K. Figure II.2 illustrates the baseline PBGA package with no thermal management.

Plastic Ball Grid Array Model with Jet Ipingment

This model involved a detailed CFD calculation based on the pressure difference, Reynolds number, and geometry of the jets. The fluid boundaries outlined the flow path of the air as it traveled from the compressor to the underside of the chip, eventually exiting out into the ambient environment. The pressure chamber mounted on the back of the PCB was assumed to be supplied with a constant gauge pressure of 15.9 kPa from the compressor. This boundary condition was not based on the pressure drop through the jet holes but on the maximum pressure the compressor can produce. The large pressure boundary condition illustrated the maximum cooling effects of high flow rate direct interconnect cooling. The pressure at the outlets of the jets was assumed to be ambient. The solder balls were represented by cylinders of the same surface area to ensure the rigidity of the mesh. Once these parameters were established, the fluid path surface boundary conditions were set.

The Reynolds number was calculated based on the maximum velocity leaving the jet orifice, the jet diameter, and the kinematic viscosity of air at 293 K. Reynolds number calculations can be found in Appendix A. Laminar flow can be considered for unconfined free jets when Reynolds numbers are below 2300 [Incorpera, 1999]. The exit velocity was found based on both the flow rate and the pressure drop. The characteristic curves of a diaphragm compressor were used in the initial modeling. The flow rate verse pressure curve, shown in Figure II.3, of the diaphragm compressor represented the flow rate the compressor produced at a given pressure drop through the jet holes. As the

compressor produced a higher pressure the flow rate decreased which affected the jet exit velocity.

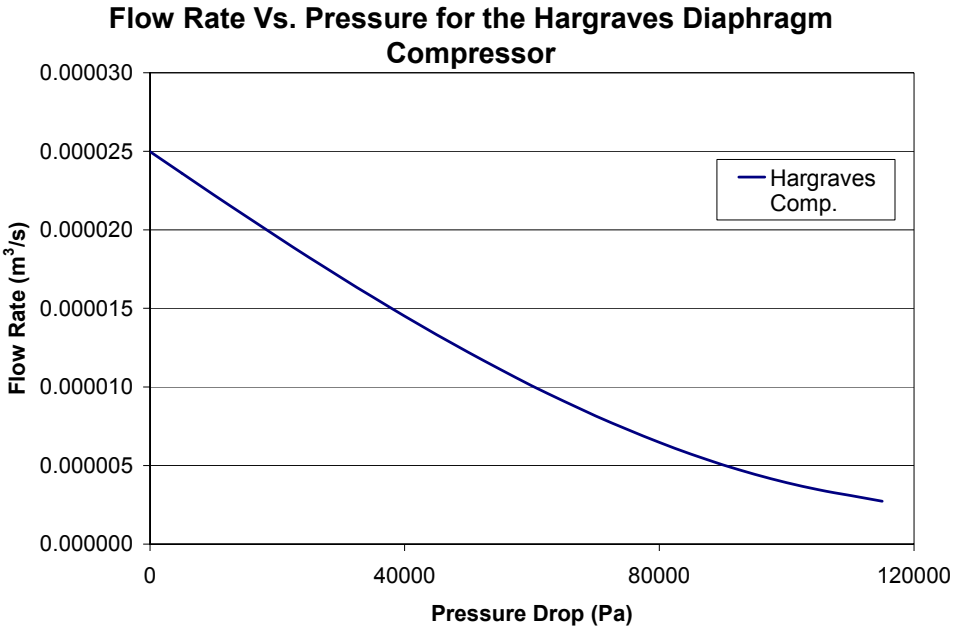


Figure II.3: The flow rate and pressure drop characteristic curve for the diaphragm compressor.

The pressure drop through the jet orifices was calculated applying the Bernoulli's equation through one hole. The pressure drop is the amount of pressure the compressor must overcome to get air to flow through the jet holes. The higher the flow rate the higher the exit velocity which allows for more heat removal. Appendix A shows the results for the Reynolds number, flow rate, pressure drop calculations for the two compressors which were used for the experiments.

The bottom of the chip was given a surface heat flux of 11,593 W/m^2 based on the percentage of heat that reached the bottom of the package due to chip level heating. This percentage was found from the results of the PBGA baseline model. The solder

balls were given a volumetric heat load of 319,482 W/m^3 based on the geometry, number of the solder balls, and heat generation described in Table II.1. The chamber tube and jet walls were given an h of 3 W/m^{2}K and an initial temperature of 398 K. The top of the PCB was given an h of 5 W/m^{2}K and an initial temperature of 300 K.

Fluent calculated an air velocity of 6 m/s on the underside of the chip. A finer mesh run was then made to ensure the predicted exit velocity was accurate. The two results based on the different mesh sizes were within 0.5 m/s of each other. The model was run once again assuming the air flow was turbulent. The calculated velocity remained around 6 m/s. The velocity calculated by Fluent was used in the ANSYS model. Figure II.4 shows the fluid path and boundaries of the Fluent model.

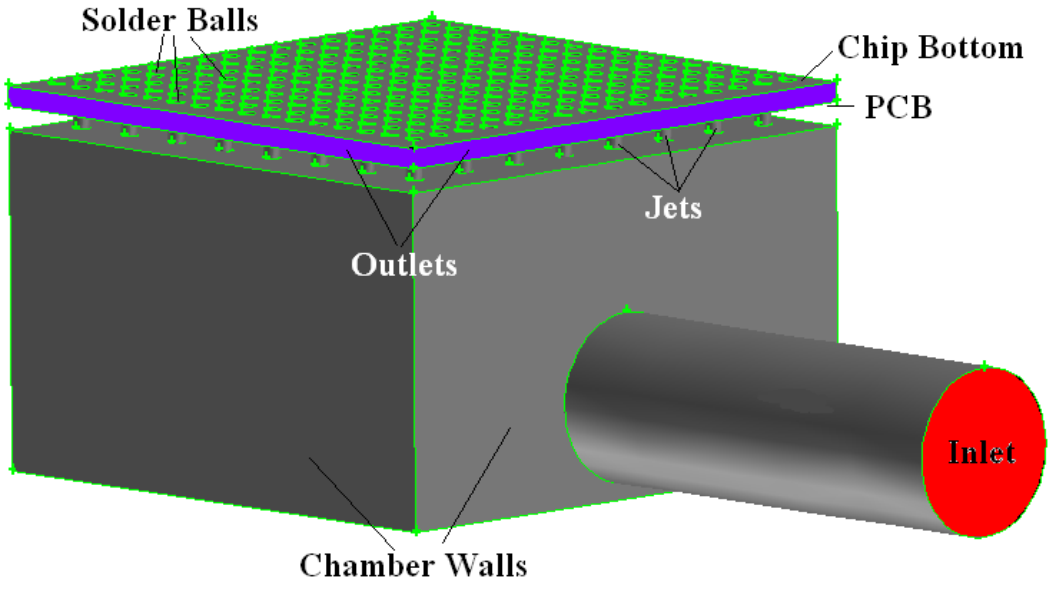


Figure II.4: The fluid path boundaries modeled in Fluent

Fluent also calculated a value for *h* that ranged from 130 W/m^{2}K to 285 W/m^{2}K for the underside of the package. The sections with the highest heat transfer coefficients were located directly above the jets. The *h* calculated for the solder balls ranged from 55 W/m^{2}K to 157 W/m^{2}K. These values were expected to be lower than the heat transfer coefficients of the underside of the package because they were not in the direct path of the air flow.

The boundary conditions calculated in Fluent were used in ANSYS to simulate jet impingement cooling on the underside of the chip and solder bumps. Convective heat transfer coefficients were set to 130 W/m^{2}K and 55 W/m^{2}K on the underside of the package and solder balls respectively. The lower *h* values were chosen to produce a conservative model. The remainder of the boundary conditions and heat loads remained the same as in the PBGA baseline model. The ANSYS model solved this system as steady state.

The model showed a drastic reduction in temperature in both the chip and solder balls. Jet impingement cooling reduced the maximum temperature by 50 K over the PBGA baseline model. The maximum temperature of the chip was 316 K and of the solder balls 315 K. The solder balls and thermal vias provided a efficient path for heat transfer. According to the model, direct cooling of the interconnects can significantly reduce the temperature of both the solder balls and chip. The temperature throughout the entire package ranged from 313 K to 316 K, which reduced the thermal gradient from 6 K to 3 K. Figure II.5 shows the temperature profile of the PBGA package with thermal management.

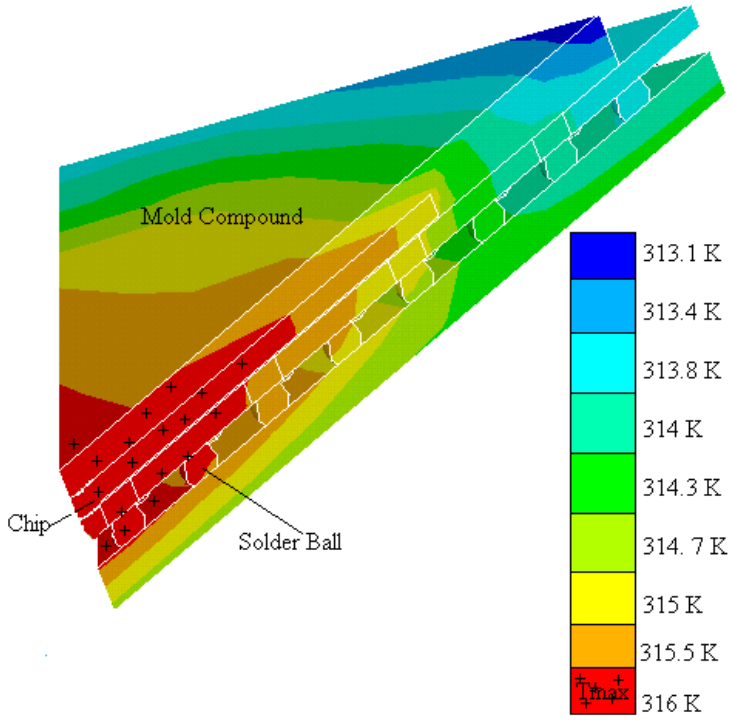


Figure II.5: The temperature profile of the PBGA package with jet impingement thermal management.

The models did not take into account several physical factors. Some of these factors include radiation and natural convection heat transfer, material properties changing with temperature, unevenly spaced heat loads, and variations in environmental conditions. The models, however, do illustrate the idea of directly cooling the interconnects of packaged chips. They show that heat can be removed from the chip through the thermal paths provided by the copper vias and solder balls. These models were a stepping stone for the experimental work illustrated in the following chapters, which will truly validate direct cooling of the off-chip metal interconnects.

CHAPTER III

INSTRUMENTATION AND EXPERIMENTAL PROCEDURES

The experiments demonstrate how effective jet impingement cooling is on a PBGA packaged IC. The temperatures of various locations throughout the PBGA package are measured while some parameters are held constant and others varied. The main objective of the experiments was to see if direct cooling of the off-chip metal interconnects was both beneficial and practical. Another important goal of the experiments was to validate the model so that then may be used to predict the effectiveness of jet impingement thermal management of other electronic architectures and using other types of cooling fluids. Also, the validated model could be used to predict the cooling effects of different jet diameters and patterns within the PCB.

The equipment used to measure and collect data is described below. Each instrument has been factory calibrated and in some cases NIST calibrated. The instrumentation uncertainty is given in the equipment manual along with a detailed description on how to set up the instrument correctly. Besides the uncertainty in the equipment some random errors were considered and included into the experimental analysis.

The experimental apparatus consists of four main segments. The first segment consists of the dummy PBGA test die. These were specially constructed chips, which were used to simulate both the chip level and solder ball heating. The second segment comprises of a specially designed PCB, which contained the jet hole designs and was used to supply the current for the Joule heating in the solder balls. The third segment consists of the air supply system. The air supply system was made up of the compressor, tubing, and pressure chamber. The final segment contains the data acquisition equipment, flow meter, thermocouples, and pressure sensor. The chip, PCB, and air supply segments are illustrated in figure III.1.

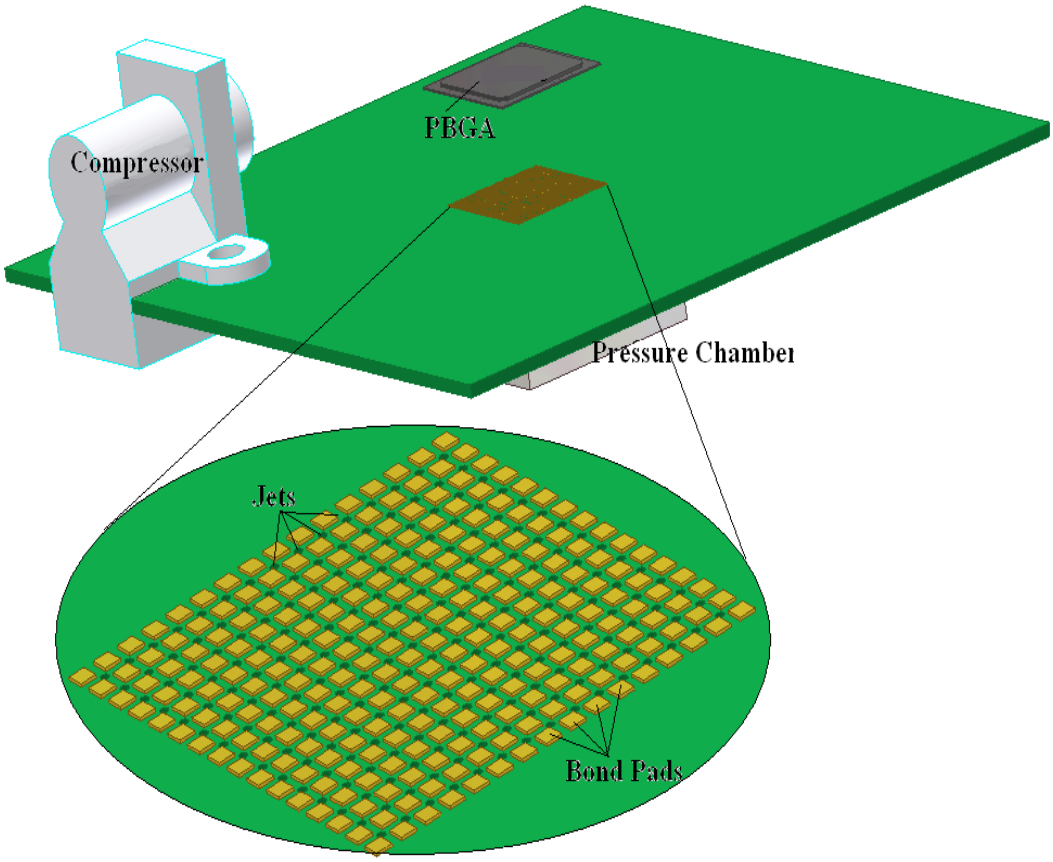


Figure III.1: The Air supply, PCB, and PGBA segments of the experimental setup.

Plastic Ball Grid Array Package Chip

A Practical Components daisy-chained PBGA package test chip was used to simulate the high power electronic component. The PBGA selected was a 17x17x1.16 mm plastic package with a solder ball pitch of 1 mm. The package contains 256 daisy chained 63Sn/47Pb solder balls which makes 128 daisy-chained pairs. The daisy chain is made of an electrically conductive metal, which will be used along with the PCB to generate Joule heating in the solder balls. The PBGA package consists of a 2-layer laminate substrate that contains both thermal and electrical vias. It also contains a 5x5x0.6 mm dummy silicon die which connects to the laminate substrate with thermally conductive grease. The silicon die does not have any wire bonds electrically connecting it to the laminate substrate.

A Minco resistive heater and K- type thermocouple were embedded into the PBGA package by QuikPac. The thermocouple lies sandwiched between the resistive heater and dummy silicon die. Figure III.2 shows the location of the resistive heater and thermocouple in the package. The 10 ohm resistive heater simulates the chip level heating which would be generated in an actual IC. The thermocouple is used to measure the temperature of the silicon die. This measurement was used to see how jet impingement cooling affected the temperature of the silicon die. Once the thermocouple and heater was in place they were encased within the plastic mold compound.

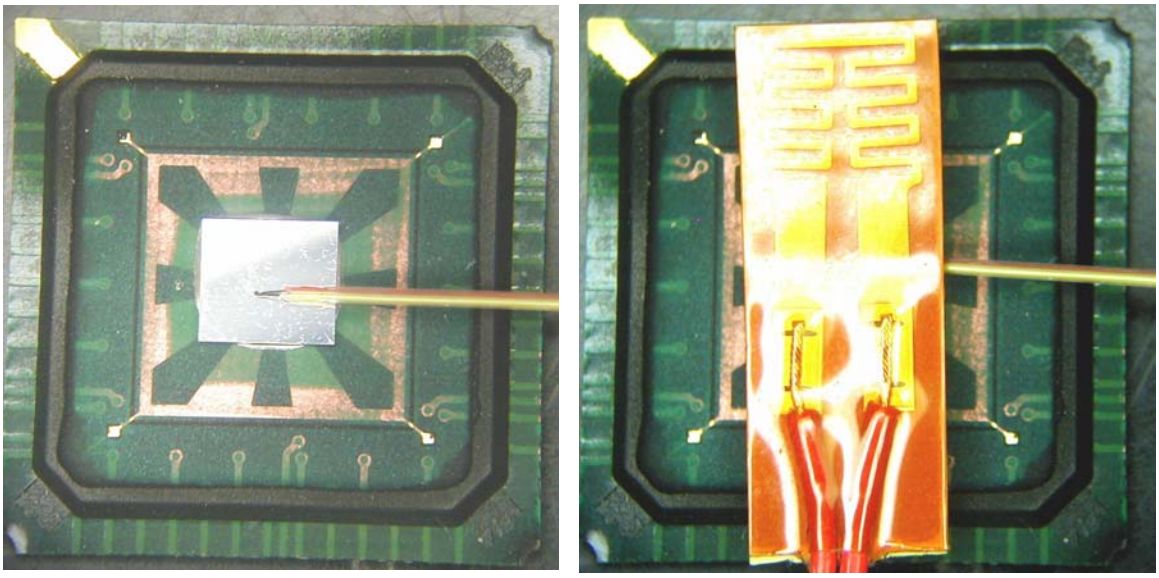


Figure III.2: The locations of the resistive heater and thermocouple in the PBGA package.

Printed Circuit Board

A PCB was fabricated to both supply current for the Joule heating in the solder balls and also contain several jet hole diameters and patterns. The PCB is a two layer board consisting of four separate circuits, which can handle large current densities. This was necessary for creating a significant amount of Joule heating in the solder balls. Each circuit contains daisy-chained bond pads corresponding to the spaces between the daisy-chained solder balls on the PBGA package.

Two jet hole patterns with two jet diameters were embedded in the PCB for impingement cooling. The nominal hole diameters were 0.250 mm and 0.368 mm. Ten jet holes for each diameter were measured under a microscope. The hole diameters ranged from 0.39 mm to 0.43 mm when the 0.368 mm drill bit was used. The hole diameters ranged from 0.31 mm to 0.35 mm when the 0.250 mm drill bit was used. The

average hole diameter for the two holes were 0.4mm and 0.32 mm with standard deviations of 0.011 mm and 0.012 mm respectively. Though the actual diameters of the 0.250 mm and 0.368 mm holes were around 0.32 mm and 0.4 mm respectively, they were still referred to as their nominal diameters throughout the rest of the paper. One pattern has all the jet holes located in the center region of the bond pads. The second pattern consists of an array of holes in the form of two diagonal lines crossing in the center of the bond pads to form an X. Appendix B contains the design pattern for the PCB and the measured jet hole diameters.

A current source meter supplied current to the PCB, which directed it through the solder ball, across the daisy chain, and back down into the PCB traveling through the entire daisy-chained solder ball pairs. The PCB and daisy-chained PBGA formed a series circuit when connected to together. This series circuit provided the Joule heating in the solder balls.

Air Supply Equipment

A custom fabricated aluminum pressure chamber was mounted with a high strength, high temperature epoxy on the backside of the PCB. The epoxy is rated at 644 K with a tensile strength of 8.1×10^7 Pa. It was also an excellent electrical insulator to electrically isolate the aluminum pressure chamber from the copper leads on the PCB. The aluminum chamber consists of two tapped holes. One connects to the compressor and the other connects to a pressure sensor. A Swagelok hose connector joins a 4.8 mm

inner diameter plastic tube to the pressure chamber. The tube links the pressure chamber to a flow meter and then the compressor.

Two commercially available compressors were used to supply the appropriate pressure differential to create flow through the jet holes. The first was a Hargraves diaphragm compressor which had dimensions of 54.1 mm x 54.6 mm x 30.0 mm and could supply a maximum pressure of 150 kPa gauge with essentially no flow rate. The maximum flow rate possible was around 5.0 x 10^{-5} m^3/s with no pressure. The diaphragm compressor was used for most of the experiments because of its size and low power consumption. The second was a Reitchle Thomas rotary compressor which had dimensions of 151.5 mm x 50.8 mm x 57.4 mm and could supply a maximum gauge pressure of 34 kPa with a flow rate of 1.7 x 10^{-5} m^3/s. The maximum flow rate possible was around 3.4 X 10^{-4} m^3/s with no pressure. The rotary compressor is not practical in portable electrical devices due to its size and power requirements. It was also much too loud to be practical in desktop computers. It did illustrate how jet impingement cooling could significantly cool the chip and solder balls with its high flow rate capability.

There are many different types and sizes of compressors available with different advantages and disadvantages. The two compressor types used in the experiments have different advantages. Diaphragm compressors tend to produce high pressures but have small flow rates. These types are useful when pushing air through very small orifices. The rotary pumps have high flow rates, but can not produce a large pressure head.

Obtaining the greatest exit velocity out of the jet holes is directly related to the flow rate; however, the flow rate has a direct relation to pressure. Each jet hole pattern and diameter has a certain pressure drop. The compressor must overcome this pressure

drop before air can flow through the hole. Whatever pressure is required has a corresponding flow rate. The higher the flow rate the higher the exit velocity. Another advantage of using compressed air was the ability to obtain cool air away from the heat sources, unlike fans and heat sinks which are surrounded by elevated air temperatures. The pressure and flow rate characteristics of the two compressors used in the experiments can be found in Appendix A.

Measurement and Data Acquisition Equipment

Five 0.152 diameter special limits Nickel/Chromium and Nickel/Aluminum (K-type) thermocouples were evenly distributed through several bond pads on the PCBs for each jet hole pattern. Four holes were drilled into the bond pads and through the FR4 material to place the thermocouples. The locations of the thermocouples are illustrated in figure III.3. The thermocouples were placed in the holes so that just the tip was exposed above the surface of the bond pad. Four thermocouples were placed in the inner periphery bond pads and one was placed in the center. They were held in place by Kapton tape which withstood the high temperature exposure during the reflow process.

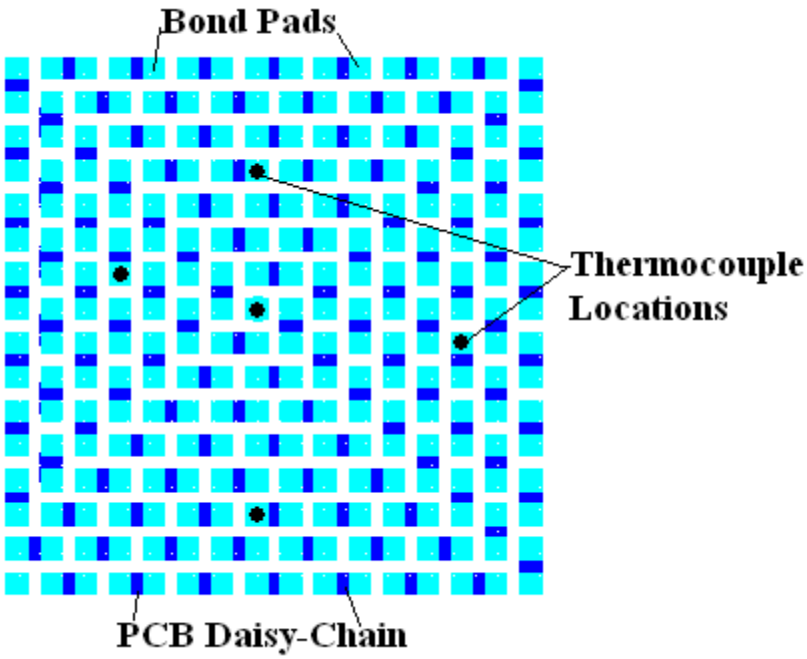


Figure III.3: The five thermocouple locations on the bond pads of the PCB which was embedded into the solder balls during the reflow process.

The Kapton tape served two purposes. It held the thermocouples in the correct position and prevented solder from entering the holes during the reflow process. The tips of the thermocouples were embedded into the solder balls during the reflow process of attaching the PBGA to the PCB. These thermocouples in conjunction with the embedded thermocouple in the PBGA package were used to obtain the temperature measurements to validate the models.

The thermocouples in the solder balls were calibrated using a high accuracy thermometer and a convection oven. The thermometer ranged from 273 K to 373 K with a 0.1 K readability. The oven was set at room temperature, 323 K, 348 K, 363 K, and 373 K and held at each temperature until the whole system had reached steady state. The system was considered steady state when the average change of the thermocouple

temperatures was less then 0.2 K over 10 minutes. Then the temperature readings of the thermometer and thermocouples were recorded.

The thermocouples' temperature measurement separated more from the thermometer reading as the oven temperature was increased. This was mainly due to the error in the electronic cold junction built into the Agilent data acquisition unit. A second order polynomial curve was fitted to the average thermocouple temperatures of a given temperature setting. An equation was extracted from this curve to adjust the thermocouple temperature measurement to be closer to the thermometer reading. Figure III.4 illustrates the fitted polynomial curve used to adjust the thermocouple measurements. The thermocouples in each of the other three experimental setups had their own unique calibration and fitted curves, which can be found in Appendix D.

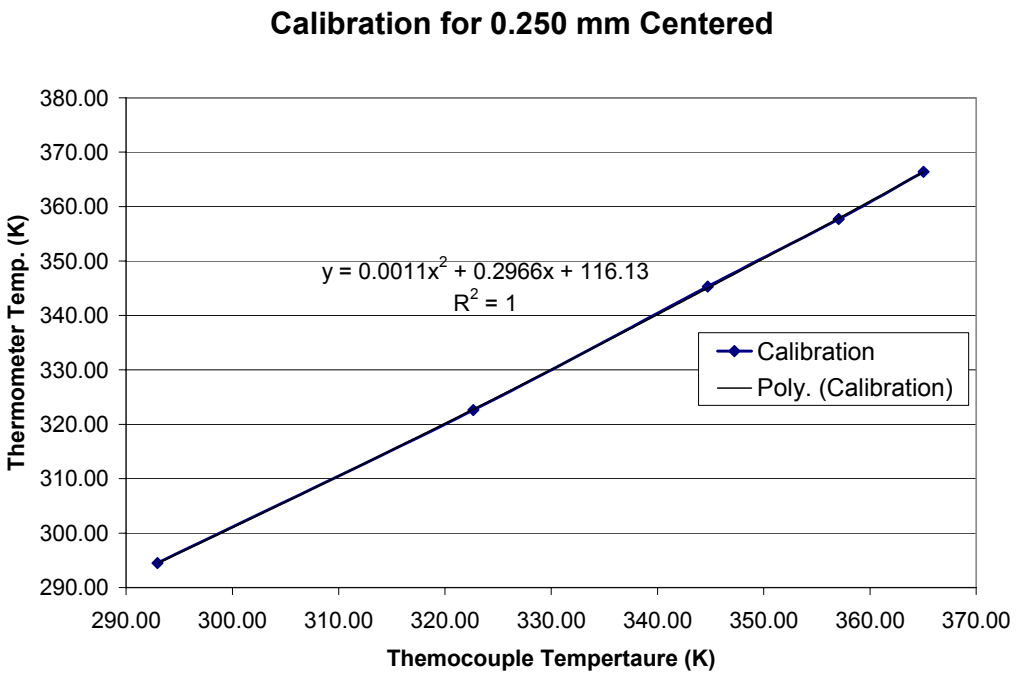


Figure III.4: The fitted polynomial curve used to adjust the thermocouple measurements to the thermometer measurements.

A Fathoms flow meter was used to measure the flow rate produced by the compressor. The flow meter was rated for a flow range of 0 to 3.4 x 10^{-4} m^3/s and is NIST traceable with an accuracy of 1% of full scale. It was connected to the compressor and also the pressure chamber through a 4.8 mm diameter plastic tube. The flow meter measured flow rates which were used to validate the model. The flow meter specifications can be found in Appendix C.

A Wika pressure transducer was used to measure the pressure in the pressure chamber. The pressure transducer had a pressure range of 0 to 34.5 kPa and an accuracy of 0.25% of full scale. It was also necessary to determine the pressure drop through the jet holes. This pressure measurement was also compared to the analytical pressure drop calculations used to conduct the initial modeling. Knowing the pressure drop will help in selecting the appropriate compressor for different jet hole geometries. A detailed description of the pressure transducer can be found in Appendix C.

Three power supplies were used to power the measurement instruments and supply current to the PCB. Two digital display Agilent power supplies that supplied up to 25 V at a maximum of 1 A were used to power the pressure transducer, flow meter, and the resistive heater embedded in the PBGA package. Each instrument required a different voltage and current setting to ensure that it functioned properly and at full capability. The PCB was powered by a more robust power supply in order to generate a significant amount of Joule heating in the solder balls. The digital display Instek power supply was capable of producing a maximum of 35 V at 10 A of current. More detailed information on these power supplies can be found in Appendix C.

An Agilent data acquisition (DAQ) switch unit connected to a computer through a general purpose interface bus (GPIB) was used to collect the data from the instruments. The DAQ switch unit was equipped with a 5 ½ digital multimeter which interpreted the output signals of the instruments. The instruments were connected to the DAQ switch unit through a 20-channel relay card outfitted with a cold junction for the K-type thermocouples. Agilent software Benchlink interpreted the data collected by the DAQ and stored it for analysis. Benchlink had the K-type thermocouple characteristics included in its programming which allowed for a direct temperature measurement in degrees Celsius. The program recorded the voltage output from the flow meters and current output from the pressure transducer. Detailed information about the Agilent DAQ can be found in Appendix C.

Experimental Parameters

The experiments tested the effectiveness of jet impingement cooling while varying several controlled parameters. These parameters included heat generation in both the chip and solder balls, jet hole diameter and geometries, and compressors. Other uncontrolled parameters such as the atmospheric pressure and temperature varied during the experiments; however, since the experiments occurred over a short amount of time these were considered negligible. The room temperature was monitored and recorded during the experiments to be assured of this assumption. Each of the controlled parameters as varied to optimize certain characteristics of jet impingement cooling. They also defined the boundary conditions used to validate the models.

The first major experimental variation was designed into the PCB. The jet hole diameters were designed into the PCB based on the solder ball pitch of the PBGA. The maximum hole diameter based on a 1 mm pitch was around 0.5 mm. This hole size was rather large and would not produce a sufficient amount of exit velocity so the two diameters chosen were 0.250 mm and 0.368 mm. The diameters could have been smaller but both the pressure drop and price per PCB would increase. The results of the preliminary analytical calculations, shown in Appendix A, indicate that these diameters were sufficient in producing high enough exit velocity to have effective cooling.

The two jet hole patterns were another experimental parameter designed into the PCB. The key to determining these patterns was to locate the most effective positioning of the jets. The first pattern had an array of 30 holes concentrated in the center of the bond pads in the PCB. Most of the chip level heating has been shown through the modeling and literature to be concentrated in the center of the package. This was an attempt to focus most of the cooling on the high heat areas of the package. The second pattern focused an array of jets across the entire bottom surface of the package. Two diagonal lines containing 15 jets each intersect in the middle to form an X. The idea behind this design was to remove some of the Joule heating generated in the peripheral solder balls. The two patterns are illustrated in figure III.5.

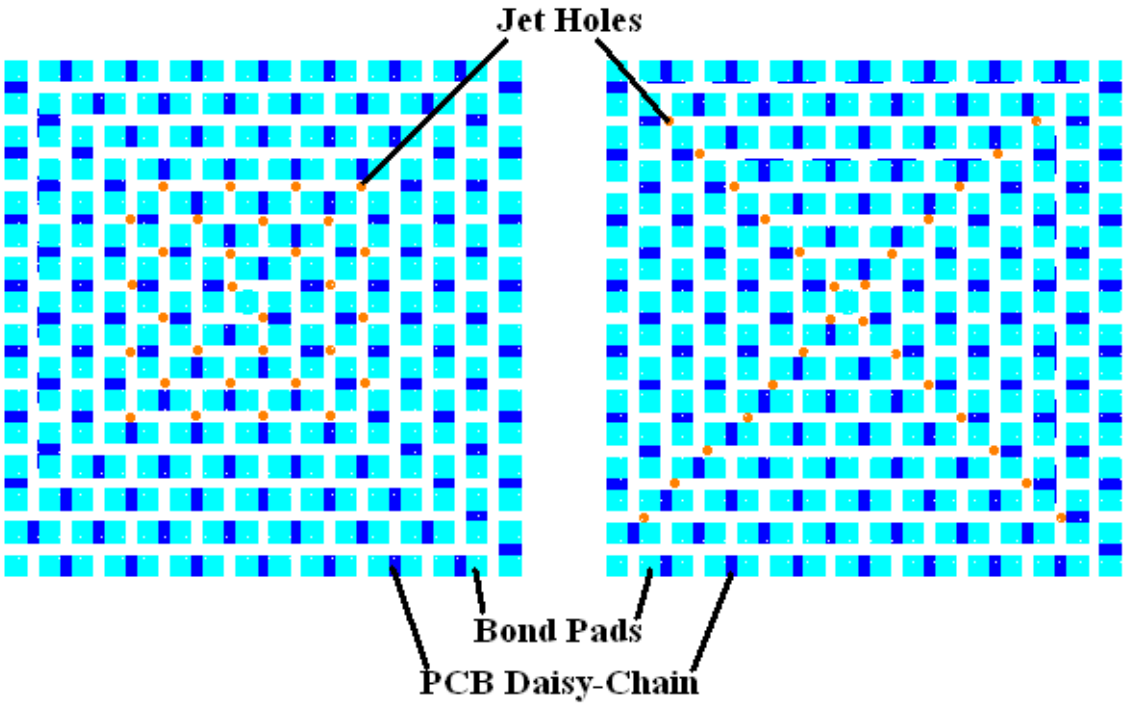


Figure III.5: The two jet hole patterns designed into the PCB.

The two compressors had different flow rate and pressure characteristics, which made them useful in different situations. The rotary compressor had a high flow rate that produced a significant exit velocity. Some draw backs of a rotary compressor were its weight and size. The diaphragm compressor had high pressure capabilities, which in turn produces smaller flow rates. This compressor was much smaller and lighter then the rotary compressor, which makes it suitable for compact and portable devices.

The main idea of using these two compressors were to see if effective cooling could be achieved with larger jet hole diameters. As the jet diameter decreases, air particles will become more of a problem. They can block various jet holes, which can reduce the heat transfer significantly. Filters could be used but add to the cost of the air supply system. The rotary compressor could produce a much higher exit velocity at

larger jet holes diameters when compared with the diaphragm compressor. Finding the optimum compressor and jet hole diameter will be important in future jet impingement cooling architectures.

The current and voltage supplied to the Minco resistive heater in the PBGA package was varied to test the effectiveness of jet impingement with different chip level heat loads. The Joule heating in the solder balls was held constant while the chip level heat was varied All the current and voltage settings for each experiment were recorded and heat dissipation was calculated based on Ohm's law, which is shown in equation I.1. Heat loads of 1, 2, 3 W were applied to the resistive heater in the PBGA and heat loads of 0.4 W and 1 W were supplied to the solder balls.

Experimental Procedure

All experiments started at room temperature, which was recorded by an external thermocouple located just outside of the compressor intake. Flow rate, chamber pressure, and temperatures were recorded for each experiment. Every precaution was taken to conduct each experiment in the same environmental parameters. Once all of the instruments were up and running, the Agilent DAQ began acquiring data. Next, the power sources were switched on and began supplying current to the solder balls for Joule heating and also to the resistive heater in the PBGA for chip level heating. Once the temperatures reached around 100 C the compressor was switched on to supply air for cooling with the exception of the experiment with a 1 W heat load. Figures III.6, III.7, and III.8 show the experimental apparatus.

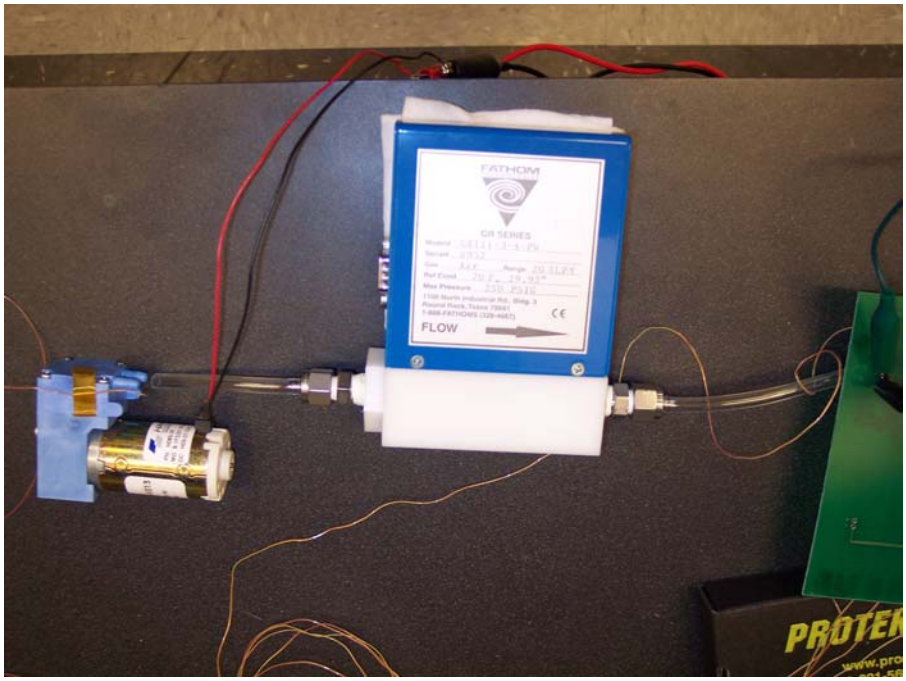


Figure III.6: The compressor (left) provides the flow rate of air used to cool the interconnects. The flow meter (center) measures the flow rate.

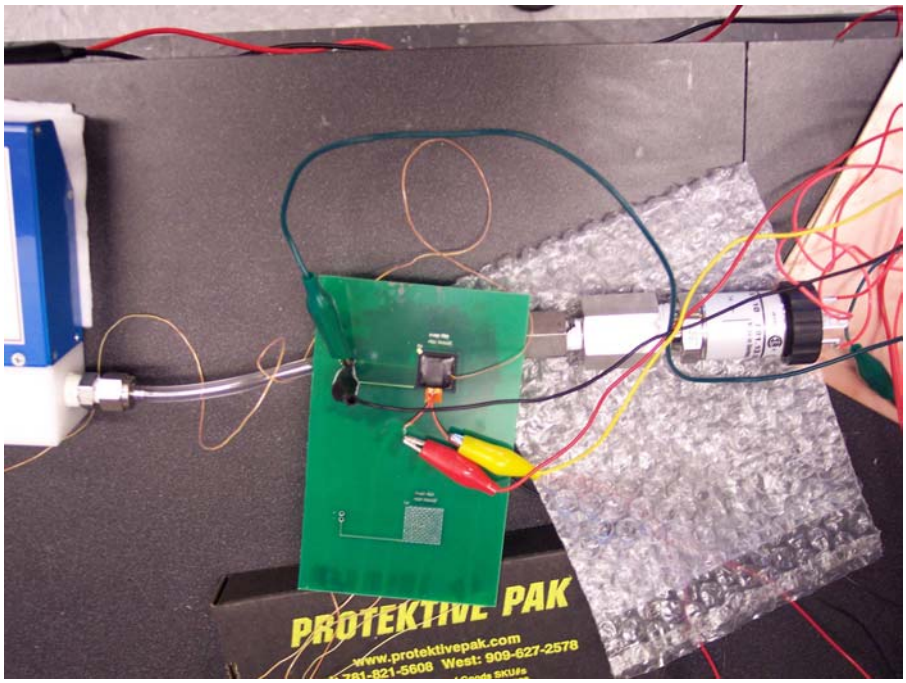


Figure III.7: The air exits the flow meter and proceeds to the pressure chamber beneath the PCB and PBGA test chip (center) where it is then

forced through the jets to cool the interconnects. The pressure is measured inside the pressure chamber by the pressure transducer (right).

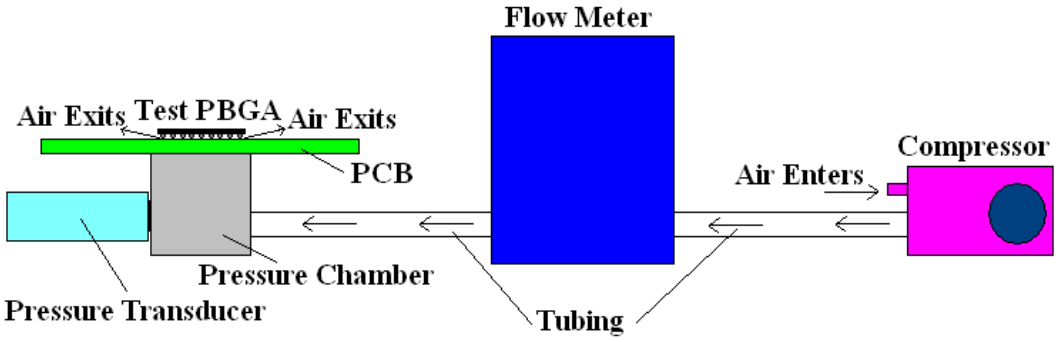


Figure III.8: The overall air flow path and experimental apparatus.

Each experiment utilized a different jet hole pattern and diameter. The BTC diaphragm compressor was used to supply air for the four jet hole architectures. The heat loads on the chip and solder balls were also varied for each hole pattern. The rotary compressor was used in several experiments with a 3 W heat load to illustrate the cooling potentials of jet impingement cooling on the bottom of the package and solder balls.

The first set of experiments involving chip heat loads of 1 W, 2 W, 3 W and a solder ball heat load of 0.4 W were run to test the effectiveness of jet impingement at different power levels. These particular heat loads were specified because of the limited temperature calibration range established with the precision thermometer. The 1 W experiments stayed with in the calibrated temperature range with only natural convection so the experiments were run for 11 minutes; 1minute at room temperature, 5 minutes of chip level and solder ball heating with no thermal management, and 5 minutes of jet impingement thermal management. The higher chip level heat loads were run for a total of 6 minutes; 1 minute at room temperature, then power was supplied to the minco heater

and solder balls until the chip temperature reached 373 K at which point thermal management was engaged.

The second set of experiments was conducted to compare top level cooling with direct interconnect cooling. A 40x40x15 mm NMB computer fan was placed directly above the PBGA package to supply top cooling. A 12 V, 1.1 A fan with a maximum flow capacity of 2.8 x 10^{-3} m^3/s was used during these experiments. The chip was supplied 1 W, 2 W, and 3 W of power, along with 0.4 W of power to the solder balls to simulate a functioning IC for each geometry. The fan was then turned on to supply cooling. The amount of time for each top level cooling experiment was identical to the interconnect cooling experiments. The temperatures of both the chip and solder balls were recorded. Figure III.9 shows the location of the fan in respect of the PBGA test package.

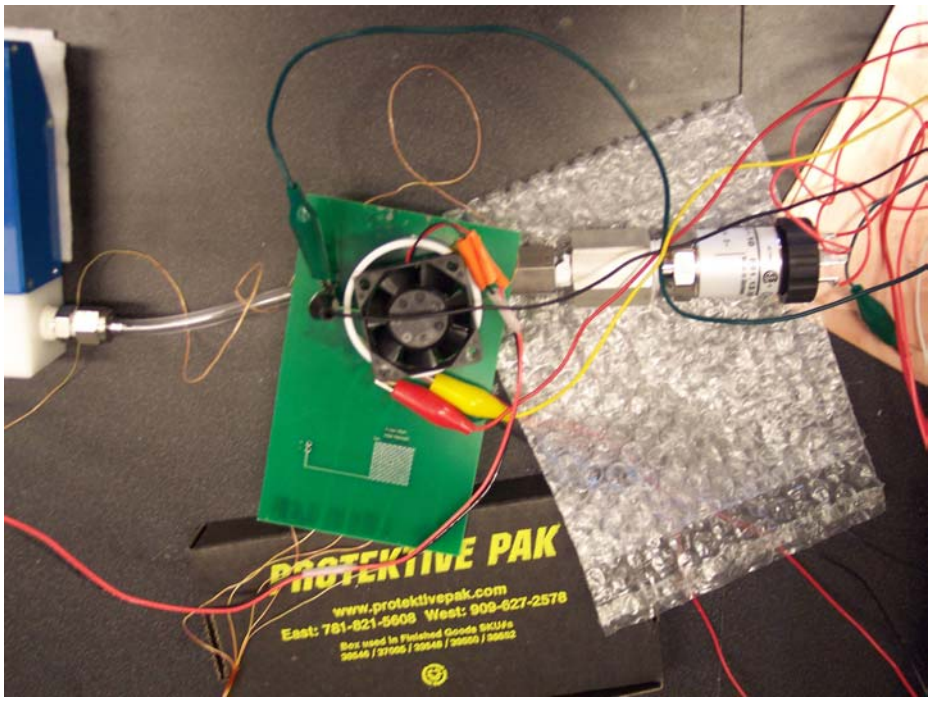


Figure III.9: The location of the top level NMB cooling fan with respect to the PBGA.

The next set of experiments involved both interconnect cooling and top level fan cooling. The chip was supplied with 3 W of power and the solder balls were supplied with 0.4 W of power. Once the chip reached 373 K both the fan and compressor were switched on to supply cooling. This was done to illustrate three-dimensional cooling. This experiment showed the best cooling out of all the other experiments. Ideally for future systems, a cooling system should be designed so that heat can be rejected from every possible dimension.

The final set of experiments involved only solder ball Joule heating. The solder balls were supplied with a current so that 1 W of power was produced. When power was supplied to the solder balls the top level cooling fan was turned to cool the solder balls. No direct interconnect thermal management was used. Next, only direct interconnect cooling was used to cool the solder balls under the same conditions. This was done to observe how effective top level cooling was on the solder balls when compared with direct interconnect cooling. All of the parameters for each experiment were summarized in Table III.1.

Table III.1: The complete list of voltage, current, and power settings for each experiment.

Experimental Procedures								
	volts	amps	Power compressor (W)					
Hargraves BTC	12	0.18	2.16					
					Vary			
	Jet Diameters (mm)	**Hole Pattern**	**Minco Heater Current (amps)**	**Minco Heater Voltage**	**Minco Heating (W)**	**Solder ball Current (amps)**	**Solder Ball and Path Voltage**	**Solder ball joule heating (W)**
	0.25	Center	0.308	3.28	1.010	1.056	0.39	0.412
	w/ only fan		0.306	3.31	1.013	1.056	0.4	0.422
			0.429	4.68	2.008	1.057	0.42	0.444
	w/ only fan		0.429	4.66	1.999	1.056	0.4	0.422
Repeat 1			0.522	5.76	3.007	1.056	0.43	0.454
	w/Fan		0.522	5.76	3.007	1.056	0.43	0.454
Repeat 1	w/ only fan		0.522	5.73	2.991	1.027	0.43	0.442
	w/Fan		0	0	0.000	1.68	0.6	1.008
			0	0	0.000	1.68	0.6	1.008
			0.428	4.67	1.999	0	0	0.000
		X	0.306	3.27	1.001	1.057	0.42	0.444
	w/ only fan		0.308	3.27	1.007	1.056	0.4	0.422
Repeat 1			0.431	4.64	2.000	1.057	0.43	0.455
Repeat 1	w/ only fan		0.434	4.62	2.005	1.057	0.42	0.444
			0.533	5.76	3.070	1.056	0.44	0.465
	w/Fan		0.529	5.76	3.047	1.056	0.43	0.454
	w/ only fan		0.529	5.68	3.005	1.057	0.43	0.455
	w/Fan		0	0	0.000	1.59	0.65	1.034
			0	0	0.000	1.58	0.65	1.027
			0.419	4.74	1.986	0	0	0.000
Repeat 1	0.3865	Center	0.31	3.25	1.008	1.035	0.37	0.383
Repeat 1	w/ only fan		0.31	3.25	1.008	1.042	0.37	0.386
			0.436	4.61	2.010	1.043	0.38	0.396
	w/ only fan		0.435	4.59	1.997	1.057	0.4	0.423
			0.531	5.65	3.000	1.03	0.39	0.402
	w/Fan		0.531	5.65	3.000	1.03	0.39	0.402
	w/ only fan		0.532	5.65	3.006	1.047	0.4	0.419
	w/Fan		0	0	0.000	1.67	0.6	1.002
			0	0	0.000	1.67	0.6	1.002
			0.432	4.61	1.992	0	0	0.000
		X	0.307	3.26	1.001	0	0	0
	w/ only fan		0.307	3.26	1.001	0	0	0
			0.43	4.61	1.982	0	0	0
	w/ only fan		0.43	4.61	1.982	0	0	0
Repeat 1			0.527	5.69	2.999	0	0	0
	w/Fan		0.527	5.69	2.999	0	0	0
	w/ only fan		0.527	5.69	2.999	0	0	0
	volts	amps	Power Compressor (W)					
Thomas Rotary	8.9	2	17.8					
	Jet Diameters (mm)	**Hole Pattern**	**Minco Heater Current (amps)**	**Minco Heater Voltage**	**Minco Heating (W)**	**Solder ball Current (amps)**	**Solder Ball and Path Voltage**	**Solder ball joule heating (W)**
	0.25	Center	0.523	5.76	3.012	1.056	0.41	0.433
	w/Fan		0.523	5.76	3.012	1.056	0.41	0.433
		X	0.529	5.76	3.047	1.056	0.41	0.433
	w/Fan		0.529	5.76	3.047	1.056	0.41	0.433
	0.368	Center	0.531	5.66	3.005	1.057	0.38	0.402
	w/Fan		0.531	5.66	3.005	1.057	0.38	0.402
		X	0.53	5.69	3.016	1.02	0.39	0.398
Repeat 1	w/Fan		0.522	5.69	2.970	1.02	0.44	0.449

CHAPTER IV

EXPERIMENTAL RESULTS AND DISCUSSION

The results of each experiment depended on many factors, some of which were controlled and others that could not be controlled. All these factors have a role in the accuracy of the measurement uncertainty. Each experiment was carried out with as much care and precision as humanly possible. A detailed description of how the fixed uncertainty was calculated can be found in Appendix E. This chapter also describes in detail the experimental geometry that provided the most effective cooling and briefly compares the results from the other three.

0.250 mm Centered Jet Hole Pattern Experiments

Today ICs are generally located in the center of the package and generate the most heat. The centered jet hole pattern focuses the cooling on the center of the package. The air impacts the bottom of the package and then spreads through the solder balls and out the gap between the packaged chip and PCB. 0.250 mm is the smallest hole that could be mechanically drilled into the PCB. Laser drilling can make holes on the order of .050 mm but is more expensive and limited to the larger PCB manufacturers. The smaller the hole the faster the exit velocity, which enhances the cooling. The trade off is

that the pressure drop increases as the hole diameter decreases. Both compressors provided sufficient pressure to over come the pressure drop through the holes. The results are in graphical form below.

The first set of results illustrates a comparison between direct interconnect cooling and top level fan cooling. The Hargraves diaphragm compressor was used for this set of experiments. The chip level heater was supplied with around 1 W, 2 W, and 3 W of power and the solder balls were supplied with around 0.4 W of power. The exact power settings can be found in appendix E under the heading "0.250 mm Centered." Figures IV.1 and IV.2 show the results of direct interconnect cooling compared to top level fan cooling with the chip level heater supplied with 1 W of power.

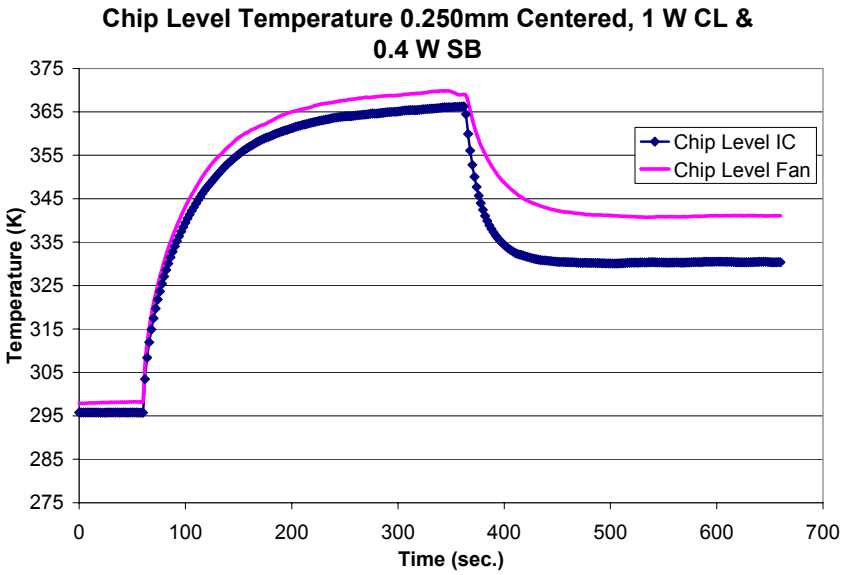


Figure IV.1: Chip level temperature for 1 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

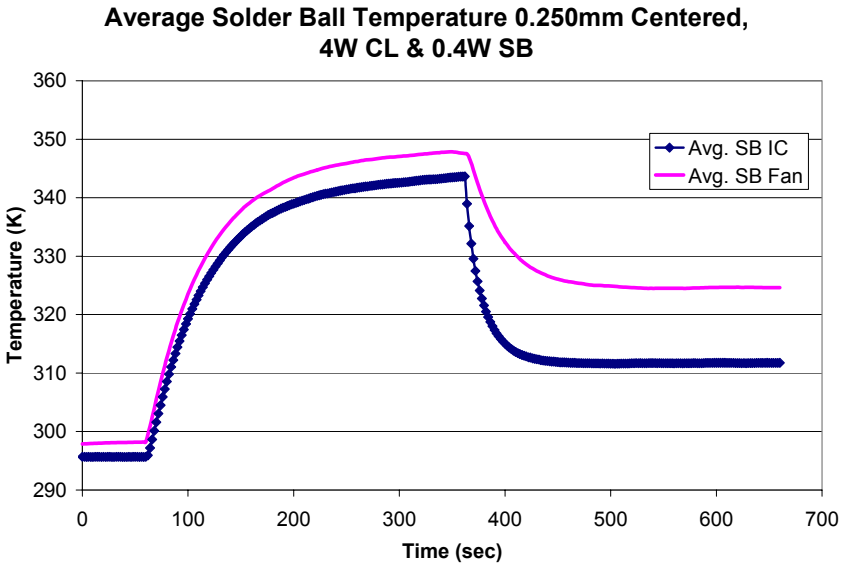


Figure IV.2: Average solder ball temperature for 1 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

These experiments lasted for 11 minutes with 1 minute at room temperature, 5 minutes of chip level and solder ball heating, and 5 minutes of direct interconnect and fan cooling. The average chip level temperature for direct interconnect cooling (IC) was 331 K and for fan cooling was 341 K. This is almost an 11 K improvement over top level fan cooling. The average solder ball (SB) temperature for direct interconnect cooling was 312 K and for top level fan cooling was 325K. This is nearly a 13 K improvement over the top level fan cooling.

The next experiments involved chip level heating of 2 W and 3 W with a constant solder ball heating of 0.4 W. These experiments were only ran for 6 minutes, each with 1 minute at room temperature and then heating was turned on until the chip level temperature reached 373 K at which point the thermal management schemes were activated. Figures IV.3, IV.4, IV.5, and IV.6 show the chip level and average solder ball temperatures for both heat settings.

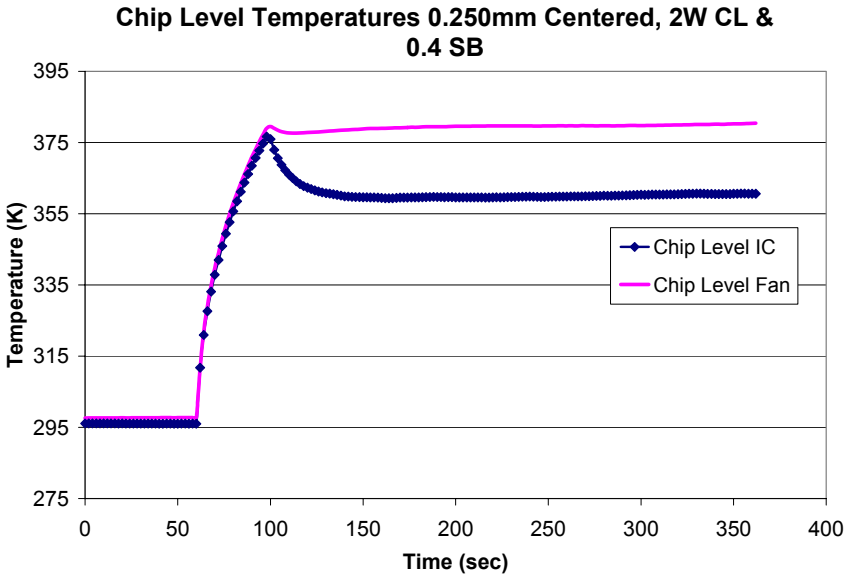


Figure IV.3: Chip level temperature for 2 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

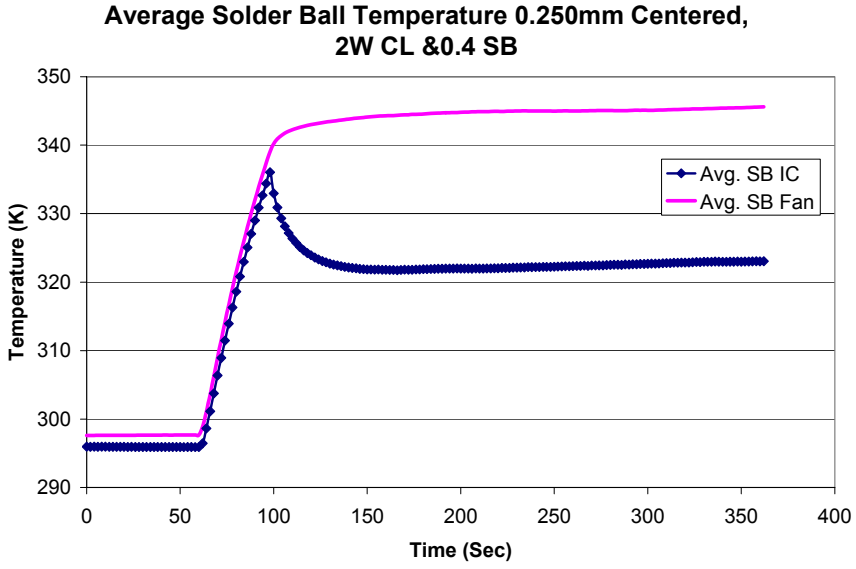


Figure IV.4: Average solder ball temperature for 2 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

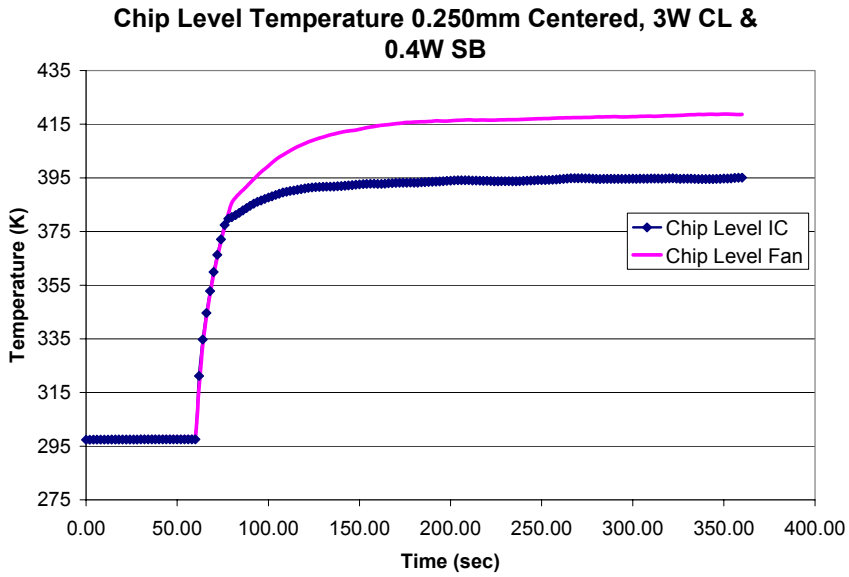


Figure IV.5: Chip level temperature for 3 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

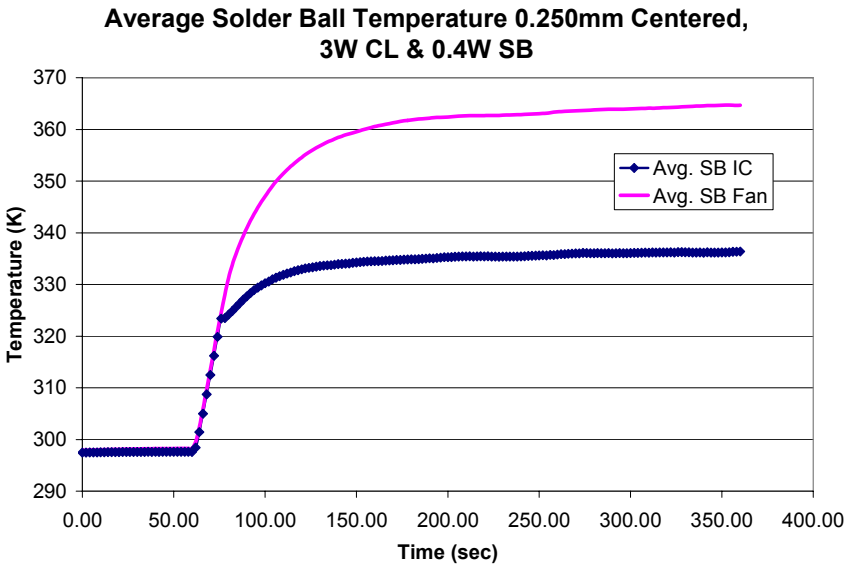


Figure IV.6: Average solder ball temperature for 3 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

The chip level temperature for direct interconnect cooling was 361 K and for fan cooling was 380 K for 2 W of chip level heating. A temperature drop of approximately

20 K was a significant improvement over top level fan cooling. The average solder ball temperature was 323 K and for fan cooling was 346 K for 2 W of chip level heating. Direct interconnect thermal management cooled the solder balls by 22 K over the fan cooling. The chip level temperature for direct interconnect cooling was 395.1 K and for fan cooling was 419 K for 3 W of chip level heating. This was more then a 23 K improvement over top level cooling. The average solder ball temperature was 336. K and for fan cooling was 365 K for 3 W of chip level heating. Direct interconnect thermal management cooled the solder balls by 28 K over the fan cooling. Each time the heat load on the chip increased the gap between temperatures for direct interconnect cooling and top level cooling increased.

The next experiments involved interconnect cooling and top level cooling together. The experiment was run with around 3 W of chip level heating and around 0.4 W of solder ball heating. The total length of the experiment was 6 minutes with 1 minute at room temperature and then the heat was applied until the chip reached 373 K, at which point both the fan and compressor were activated. Figures IV.7 and IV.8 show chip level and average solder ball temperatures respectively for only interconnect cooling and both top level and interconnect cooling.

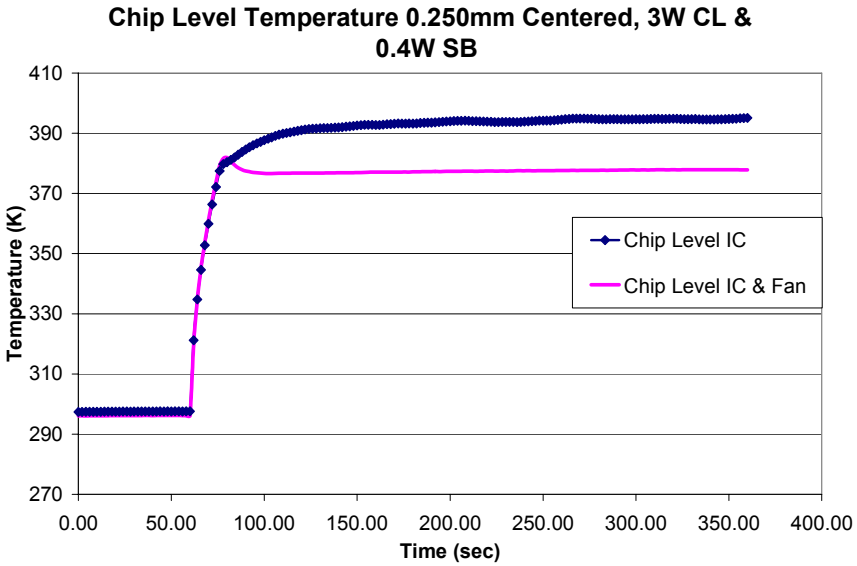


Figure IV.7: Chip level temperature for 3 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

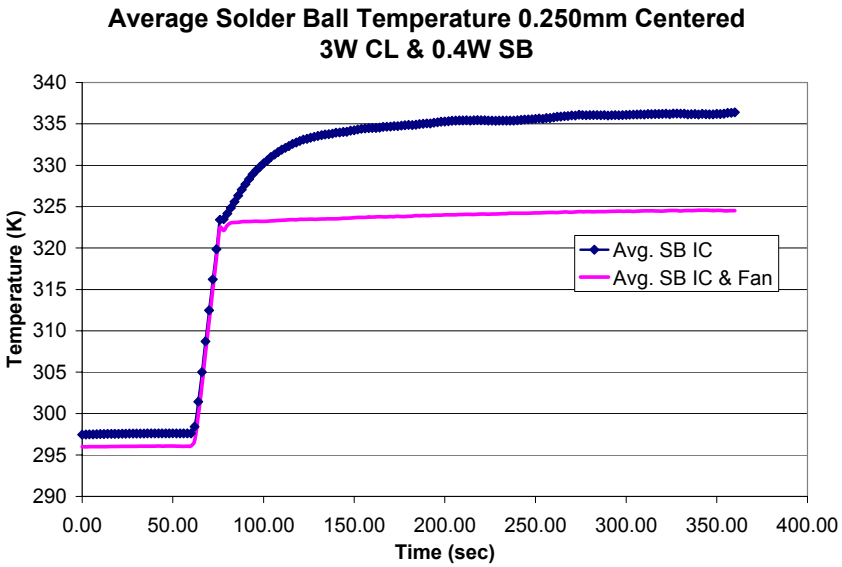


Figure IV.8: Average solder ball temperature for 3 W supplied to the chip level heater and 0.4 W supplied to the solder balls.

The abbreviations in the key box to the left of the graphs represent average solder ball with interconnect cooling (Avg. SB IC) and average solder ball with both

interconnect cooling and top level fan cooling (Avg. SB IC & Fan). The chip level temperature when both interconnect cooling and top level fan cooling were activated was 378 K, which was 16 K over just interconnect cooling. The average solder ball temperature when both interconnect cooling and top level fan cooling were activated was 225 K, which was 12 K over just interconnect cooling. Utilizing a three-dimensional cooling system greatly improved heat removal from both the chip and solder balls.

The next experiment had only a 1 W heat load on the solder balls. The experiments were run for 11 minutes with 1 minute at room temperature, 5 minutes of solder ball heating, and 5 minutes of thermal management. The experiments were run with only direct interconnect cooling and only fan cooling for comparison. Figures IV.9 and IV.10 illustrate the chip and average solder ball temperatures during the experiments.

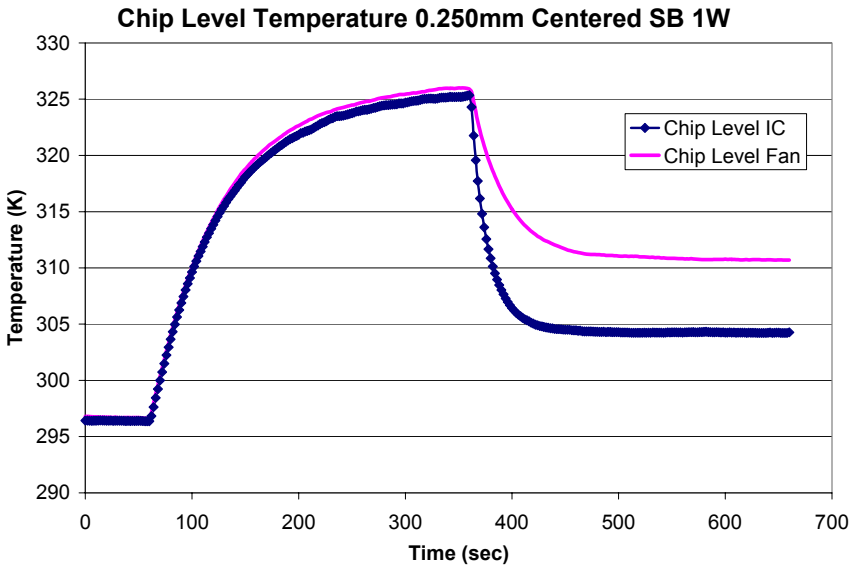


Figure IV.9: Chip level temperature for 1 W of power supplied to the solder balls.

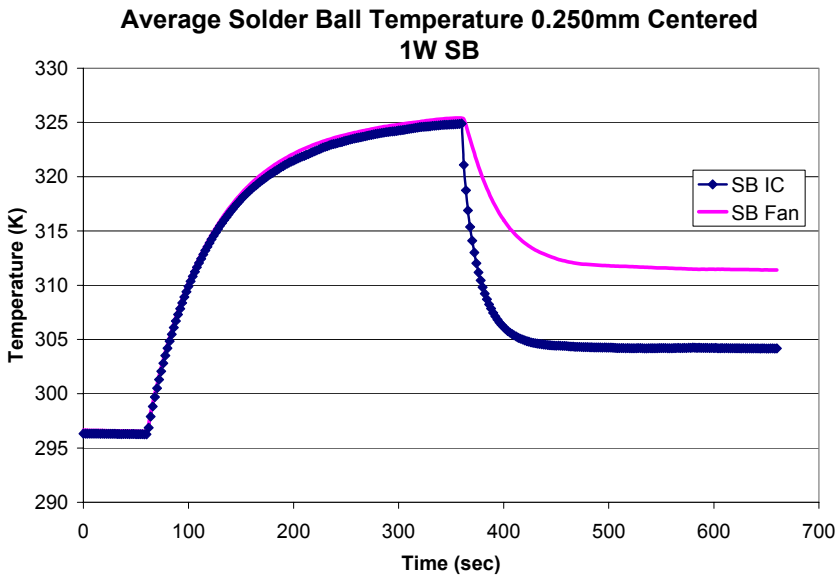


Figure IV.10: Average solder ball temperature for 1 W of power supplied to the solder balls.

The chip level temperature with interconnect cooling was 304 K and for fan cooling it was 311 K. Interconnect thermal management cooled the chip by 6 K over top level fan cooling. The average solder ball temperature with interconnect cooling was 304 K and for fan cooling it was 311 K. Interconnect thermal management cooled the chip by 7 K over fan cooling. The PBGA package had a relatively uniform temperature profile with only solder ball heating. The difference between the chip level and solder ball temperatures were very close. This was due to even heating across the entire bottom of the package, whereas when chip level heating was present all of the heat was concentrated in the middle of the package.

The diaphragm compressor was used for all of the above experiments. The pressure in the chamber and flow rate from the compressor were monitored and recorded for each experiment. The standard deviation was calculated for all the flow rate and pressure measurements for the experiments with the varying chip level heat load. The

standard deviation for pressure was calculated to be 41.3 Pa which was well within the error of ± 104.68 Pa for the pressure transducer. The standard deviation calculated for flow rate was 2.51×10^{-7} m^3/s which was slightly outside of the error of ± 2.56×10^{-8} m^3/s for the flow meter. This was probably due to voltage and current fluctuation in the compressor as it heated up from operation. The average gauge pressure for all three tests was 1093 Pa and the average flow rate for all three tests was 7.7×10^{-6} m^3/s. Figures IV.11 and IV.12 illustrate the fluctuation in the pressure and flow rate measurements for three separate experiments.

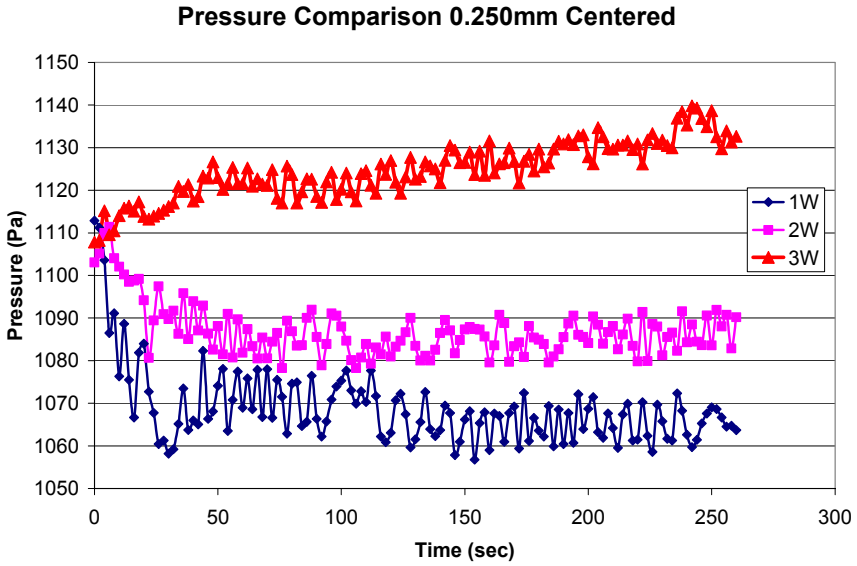


Figure IV.11: Pressure curves for three separate chip level heat load experiments obtained with the Hargraves diaphragm compressor

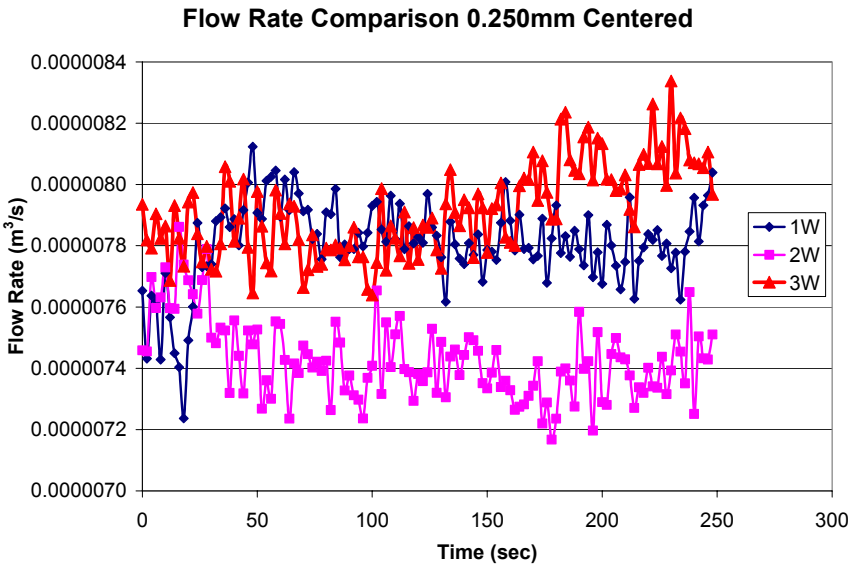


Figure IV.12: Flow rate curves for three separate chip level heat load experiments obtained with the Hargraves diaphragm compressor

The diaphragm compressor has a very small flow rate, which greatly reduces its cooling capabilities. The rotary compressor provided a much higher flow rate and was able to cool both the chip and solder balls more effectively. An experiment was run to test how much improvement in cooling the rotary compressor had over the diaphragm compressor when compared to only top level fan cooling. The chip was given a heat load of 3W and the solder balls were given 0.4 W. The experiment lasted 5 minutes with 1 minute at room temperature and then the heating was switched on. Once the chip level temperature reached 373 K the rotary compressor was activated. Figure IV.13 and IV.14 illustrate the chip level and solder ball temperatures as a result of the only rotary compressor and only top level cooling.

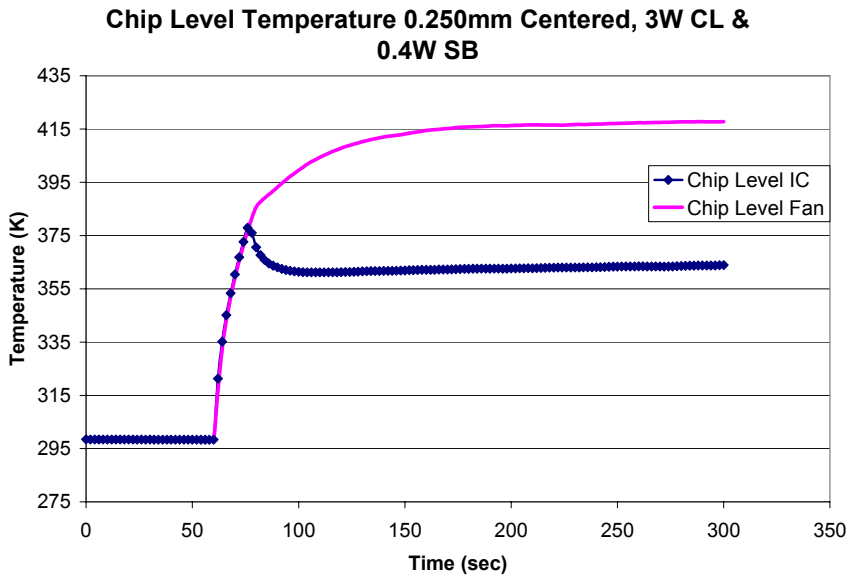


Figure IV.13: Chip level temperature for 3 W of power supplied to the chip and 0.4 W supplied to the solder balls.

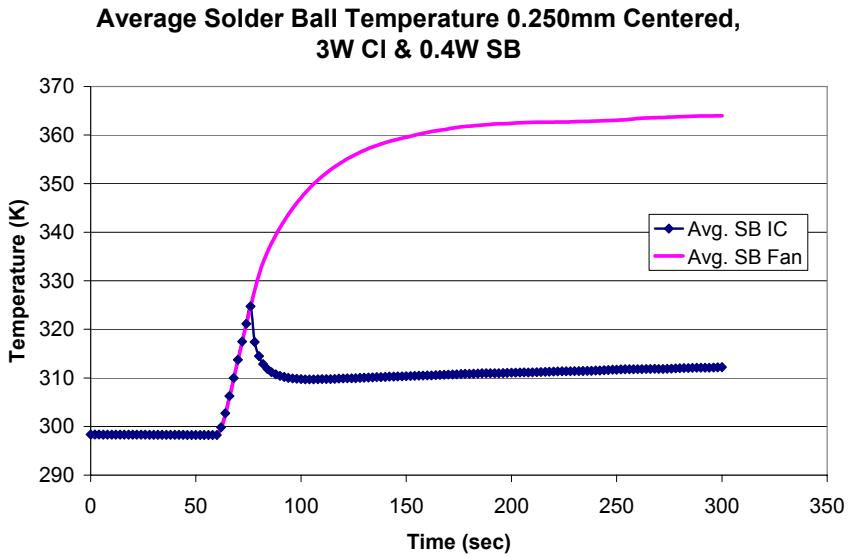


Figure IV.14: Average solder ball temperature for 3 W of power supplied to chip and 0.4 W supplied to the solder balls.

The rotary compressor cooled the chip to 363.9 K, which was 54 degrees cooler then when only top level fan cooling was used. This chip level temperature was also 32

K cooler when compared with the diaphragm compressor cooling results. The solder balls were cooled to 312 K, which was 51 K cooler then top level fan cooling. The rotary compressor cooled the solder balls by 24 K over the diaphragm compressor. This was a great example of the capabilities of direct interconnect cooling. Even though the cooling capacity of this rotary compressor was very high, it still has many draw backs that make it impractical for use in microelectronics.

The final experiment for this particular jet hole diameter and pattern was the repeatability of the temperature measurements. Two experiments with the diaphragm compressor were run with the same parameters to see how close the temperatures were. The experiment with 3 W chip level and 0.4 W solder ball heat loads with only direct interconnect cooling using the diaphragm compressor was duplicated. Figures IV.15 and IV.16 show the temperatures of the chip and solder balls for both experiments.

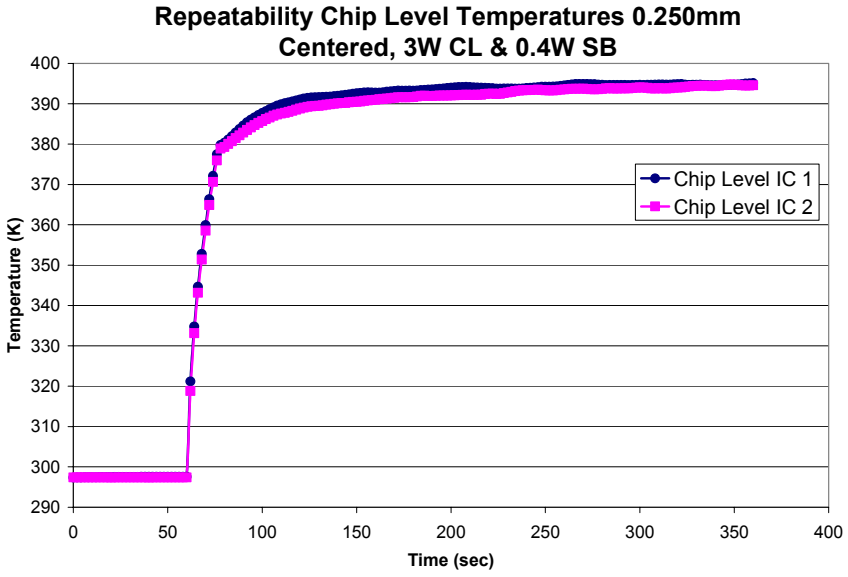


Figure IV.15: Repeatability for chip level temperatures for 3 W of power supplied to the chip and 0.4 W supplied to the solder balls.

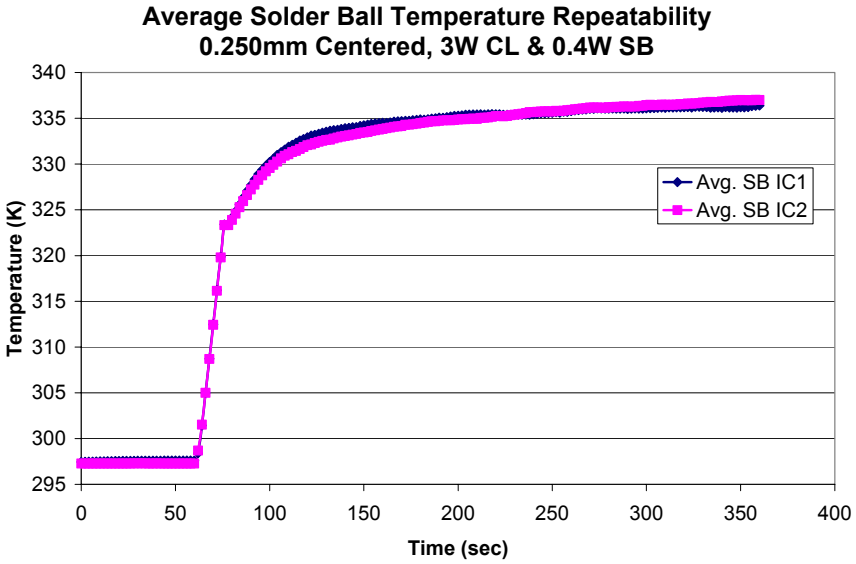


Figure IV.16: Repeatability for average solder ball temperatures for 3 W of power supplied to chip and 0.4 W supplied to the solder balls.

The maximum unbiased standard deviation for the chip level temperature was 1.7 K once the compressor was activated. The maximum unbiased standard deviation for the solder balls was 2.1 K once the compressor was activated. Both the chip and solder ball standard deviations were well within the error of ± 2.1 K for the thermocouple.

Comparisons between the Four Jet Hole Designs

The same set of experiments were run for the three other jet hole diameters and patterns. The three geometries included; a 0.250 mm jet hole diameter in a pattern of an X, a 0.368 mm jet hole diameter in a centered pattern, and a 0.368 mm jet hole diameter in a X pattern. The X pattern offered cooling to the peripheral solder balls and package. The larger jet diameters had less pressure drop so the compressor produced a higher flow

rate. Since the jet diameter was larger the exit velocity decreased. There was an optimum jet hole diameter for a given pitch size.

Each of the four experimental setup consisted of different chip level heaters, thermocouples, thermocouple locations, PBGA packages, PCB, and PBGA attachment characteristics. The same type of resistive heaters were placed into the PBGA package but slight variations in position made the chip level heating different between each experiment. Also, each solder ball path was unique to each experiment because of the possibility of defects during the reflow process. The thermocouples were placed under the same solder balls for all the experiments, but the exact location in or under the solder ball could not be confirmed. Each of these differences and uncertainties made it difficult to compare the four geometries directly.

The main discrepancy between the four experimental setups was the mold compound that incased the heater, thermocouple, and silicon die. The PBGA dummy packages were altered to house the heater and thermocouple. The thickness of the mold compound varied from test chip to test chip. This greatly reduced the capability of comparing the four jet hole diameters and patterns. These insights were based on the repeatability of various experiments conducted for each of the four jet hole designs.

The first set of experiments that showed reasonable repeatability were when only solder ball Joule heating was used. These experiments compared top level fan cooling and interconnect cooling with 1 W of power supplied to the solder balls. Only three of the four patterns could be compared because the 0.368 mm X experiments had no solder ball joule heating. Figures IV.17 and IV.18 show these experimental results for three of the four hole diameter and patterns.

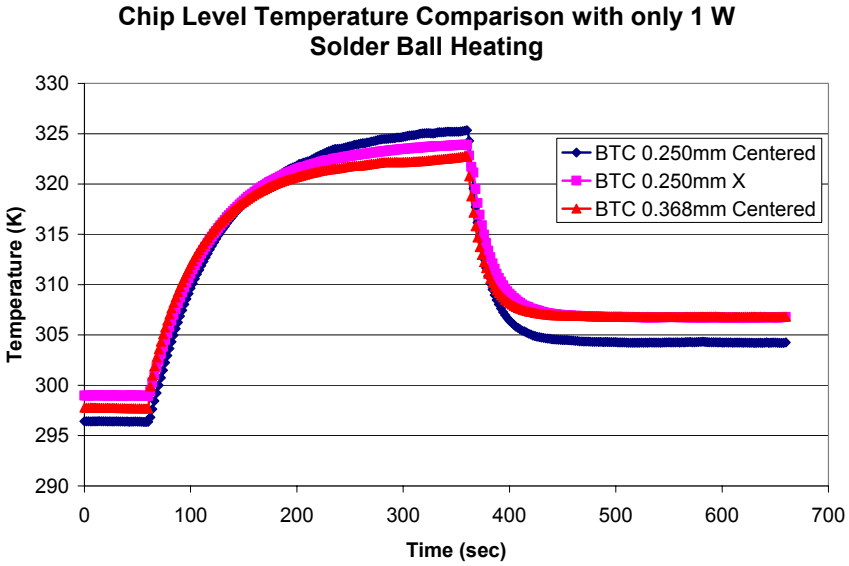


Figure IV.17: Chip level temperature differences for the four experimental setups with only 1 W solder ball heating.

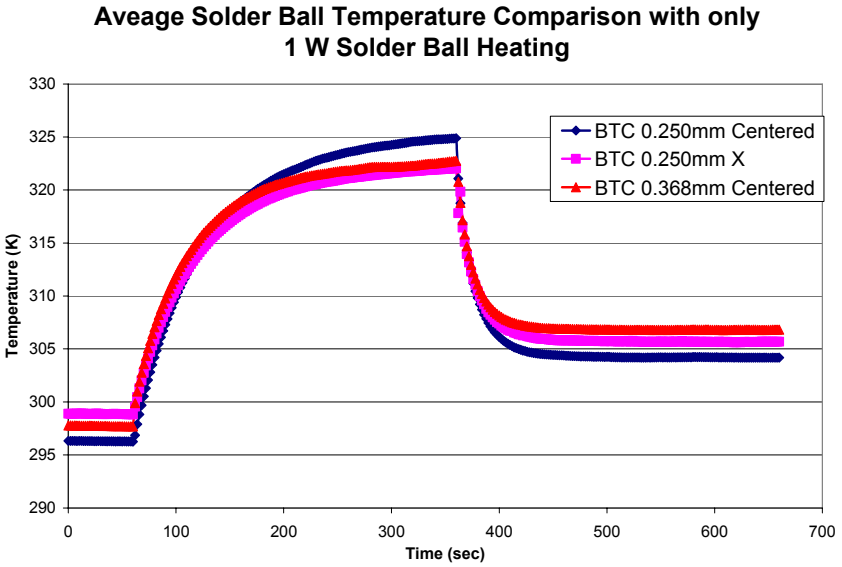


Figure IV.18: Average solder ball temperature differences for the four experimental setups with only 1 W solder ball heating.

The largest unbiased standard deviation between all three experimental designs was 1.9 K for the chip temperature, and 1.8 K for the average solder ball temperature. This indicated that the solder ball Joule heating was rather uniform between the experiments. These results also showed the most effective jet hole diameter and pattern was the 0.250 mm centered design with a 2.5 K improvement over the 0.250 mm X pattern and a 1.5 K improvement over the 0.368 mm centered pattern for chip level temperatures. The 0.250 mm centered design showed a 1.5 K improvement over the 0.250 mm X pattern and a 2.5 K improvement over the 0.368 mm centered pattern for solder ball temperatures.

The next experimental comparison between the four jet impingement designs was the measured flow rates and pressures. These were unique between each experimental jet hole geometry, however, they were very repeatable within the experiments conducted on the same jet design. Tables IV.1 and IV.2 show the average pressure and flow rate measurements for each of the four experimental jet geometries.

Table IV.1: Pressure measurements for the four experimental designs.

Experimental Design	Measured Gauge Pressure (Pa)			Unbiased Standard Deviation	Pressure Gauge Error
	1 W	2 W	3 W	Pa	Pa
0.250mm Centered	1068.82	1087.07	1124.78	41.42	100
0.250mm X	1002.00	1029.31	1055.73	39.56	100
0.368mm Centered	1103.37	1122.94	1141.82	37.85	100
0.368mm X	805.13	821.03	838.89	32.40	100

Table IV.2: Flow rate measurements for the four experimental designs.

Experimental Design	Measured Flow Rate (m^3/s)			Unbiased Standard Deviation	Flow Rate Error
	1 W	2 W	3 W	m^3/s	m^3/s
0.250mm Centered	$7.81x10^{-6}$	$7.43x10^{-6}$	$7.91x10^{-6}$	$2.51x10^{-7}$	$2.56x10^{-8}$
0.250mm X	$7.49x10^{-6}$	$7.68x10^{-6}$	$7.88x10^{-6}$	$2.21x10^{-7}$	$2.56x10^{-8}$
0.368mm Centered	$8.17x10^{-6}$	$7.68x10^{-6}$	$7.74x10^{-6}$	$2.60x10^{-7}$	$2.56x10^{-8}$
0.368mm X	$7.26x10^{-6}$	$7.60x10^{-6}$	$7.97x10^{-6}$	$3.36x10^{-7}$	$2.56x10^{-8}$

The tables show that both the standard deviation of the flow rate and pressure measurements are well within the error of the instruments. The smallest pressure drop measured was with the 0.368 mm X pattern. The other three experimental designs had similar pressure drops. The flow rates were similar among the four designs. These results indicate that both the flow rate and pressure drop did not contribute to the variations between the four experimental setups.

Another parameter that could contribute to the significant temperature differences between each experimental design was the repeatability of the temperature measurements. The experiments performed on each jet hole geometry had very good repeatability. At least one experiment was repeated for each of the jet hole geometries in order to verify the effectiveness of the thermal management scheme. For the 0.250 mm centered jet hole design the 3 W chip level and 0.4 W solder ball heating experiment was repeated. For the 0.250 mm X jet hole design the 2 W chip level and 0.4 W solder ball heating was repeated. For the 0.368 mm centered jet hole design the 1 W chip level and 0.4 W solder ball heating experiment was repeated. For the 0.368 mm X jet hole design

the 3 W chip level heating experiment was repeated. The temperature measurement standard deviation and error are shown in the table IV.3 for each of the four experimental designs.

Table IV.3: Temperature repeatability among the experiments for each of the four jet hole designs at various chip level heat loads.

Experimental Design	Average Chip Level Temperature Measurements (K)						Unbiased Standard Deviation	Thermocouple Error
	1 W	1 W repeat	2 W	2 W repeat	3 W	3 W repeat	K	K
0.250mm Centered	NA	NA	NA	NA	395	395	1.7	2.1
0.250mm X	NA	NA	360	360	NA	NA	0.5	2.1
0.368mm Centered	326	327	NA	NA	NA	NA	0.5	2.1
0.368mm X	NA	NA	NA	NA	373	374	1.0	2.1
	Average Solder Ball Temperature Measurements							
0.250mm Centered	NA	NA	NA	NA	336	337	2.1	2.1
0.250mm X	NA	NA	326	326	NA	NA	0.5	2.1
0.368mm Centered	314	315	NA	NA	NA	NA	0.4	2.1
0.368mm X	NA	NA	NA	NA	335	335	0.8	2.1

Each chip heat load of 1 W, 2 W, and 3 W also had a 0.4 W solder ball heat load. The chip level and solder ball temperatures shown were averaged after jet impingement cooling was initiated and the PBGA test package had reached steady state. The repeatability between the experiments using the same test die was well within the uncertainty of the thermocouples. This indicates the thermocouples and thermal management system were working properly and consistently.

The only other uncertainty was in the heater, thermocouple, and silicon die embedded in the mold compound. The temperatures between the four experimental designs could not be compared directly because of the uncertainty in the location of the components embedded in the mold compound. The only way the temperatures of each experimental design could be compared was looking at a temperature difference.

Each experimental setup underwent the same tests, with the exception of the 0.368 mm X setup. This particular set up did not have solder ball heating for any of the tests with the diaphragm compressor. When the PBGA package reached a certain temperature, the solder ball path resistance increased so much that it acted as an open circuit. Thus no joule heating was created in the solder balls for that particular experimental setup. Despite this fact, the temperature difference of the 0.368 mm X setup was still compared to the others for the same reasons the other experimental sets can be compared.

Heat loads of 1 W , 2 W, 3 W were supplied to the chip with a constant 0.4 W supplied to the solder balls. The experiments were run with the diaphragm compressor providing the interconnect cooling and then with top level fan cooling. The temperature difference between the two cooling schemes was compared among each experimental setup. Figure IV.19 and IV.20 show the temperature difference for the chip and solder balls for each jet hole diameter and pattern.

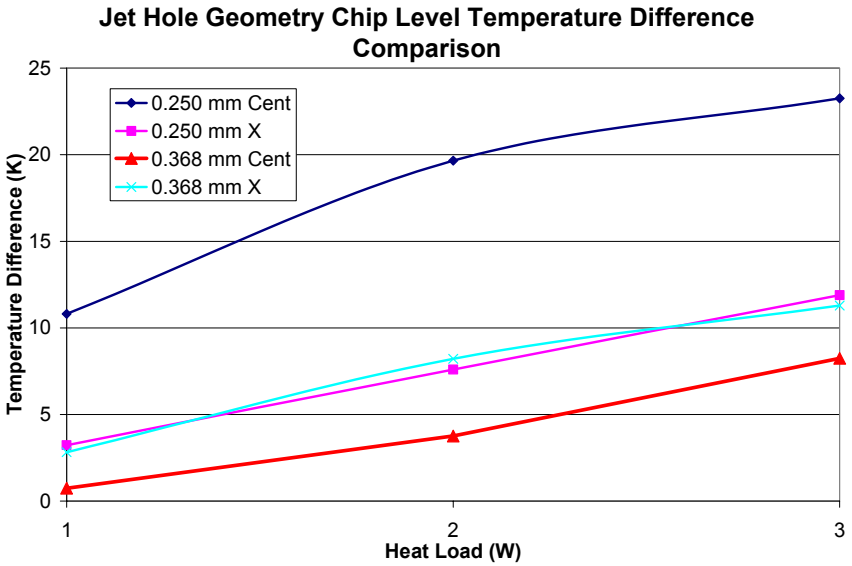


Figure IV.19: Chip level temperature difference between fan cooling and interconnect cooling for the four experimental setups.

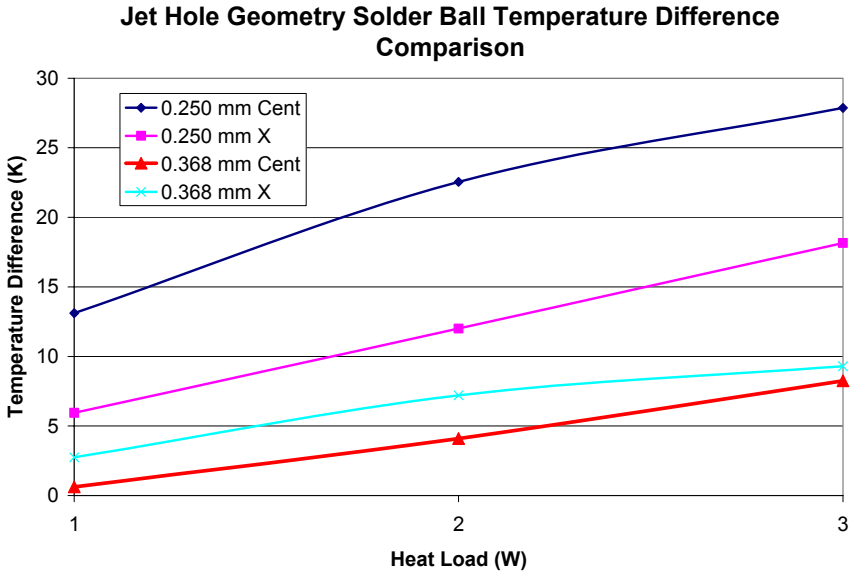


Figure IV.20: Average solder ball temperature differences between fan and interconnect cooling for the four experimental setups.

The data clearly show that the 0.250 mm jet hole diameter centered pattern was the most effective cooling geometry with a chip level temperature difference of 11 K over

the second most effective. The second best was the 0.250 mm jet hole diameter X pattern. The third best was the 0.368 mm jet hole diameter X pattern followed by the 0.368 mm jet hole diameter centered pattern. According to the experimental data the effectiveness of the cooling was more dependant on the hole diameter then on the hole pattern. All four geometries showed an improvement in cooling as the chip level heat was increased.

The next comparison between the four jet hole geometries was using the rotary compressor to supply the air for direct interconnect cooling. All four geometries were supplied with a 3 W chip level and 0.4 W solder ball heat load. Once again the temperature difference between interconnect cooling and top level fan cooling was compared. Figure IV.21 illustrates the temperature difference for the chip and solder balls for each jet hole diameter and pattern.

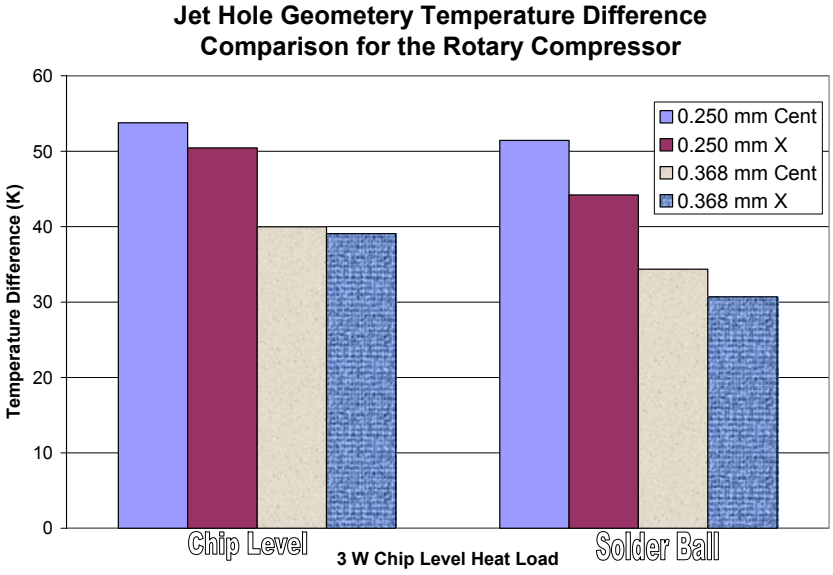


Figure IV.21: Chip level and average solder ball temperature differences for the four experimental setups using the rotary compressor.

Once again the most efficient cooling pattern was the 0.250 mm jet hole diameter centered pattern with only 2.5 K above the next best. The larger jet hole diameter experimental setups were less effective. The temperature difference trends for the rotary compressor follow along with that of the diaphragm compressor with the exception of the 0.368 mm centered pattern being slightly more efficient then the 0.368 mm X pattern. The data from the experiments using both the diaphragm and the rotary compressors conclusively show a smaller hole diameter was the one parameter that had the greatest effect on cooling.

Another important comparison was the power consumption between each of the three cooling devices. The fan ran at 12 V and 0.1 A which gave a total of 1.3 W of power consumption. The diaphragm compressor operated at 12 V and 0.18 A, which gave a total of 2.1 Amps. The rotary compressor ran at 12 V and 2 A, which gave a total of 24 W of power consumption. The rotary compressor produced the best cooling results but consumes significantly more power. This makes it the most impractical candidate for use in cooling microelectronics. The diaphragm compressor consumes 61 % more power over the fan but cools both the chip and solder balls more effectively. Decreasing the operating temperature of both the chip and solder balls a few degrees can greatly increase mechanical and electrical reliability of the packaged IC.

CHAPTER V

NUMERICAL MODELING BASED ON EXPERIMENTAL RESULTS

Numerical simulations were developed modeling the four jet hole designs. Since, there were many uncertainties between each of the four experimental apparatuses, the model was adjusted to fit only the 0.250mm centered jet hole design. The other three models had the same PBGA geometry, material properties, and the same heat loads which made everything uniform between the models with the exception of the jet hole diameters and patterns. This was done to allow a direct temperature profile comparison between all of the four jet hole designs.

Model Description

The air covection and conduction models were constructed completely in Fluent. Only ¼ of the PBGA package was modeled to reduce computational time. The PBGA package consisted of a silicon die, chip attach material, laminate substrate, copper vias, 63Sn/37Pb solder balls, and mold compound. The PBGA was attached to a PCB board which contained the jet hole geometries. The pressure chamber, jet holes, and space

above the package were considered the air path. Figure V.1 illustrates the model geometry.

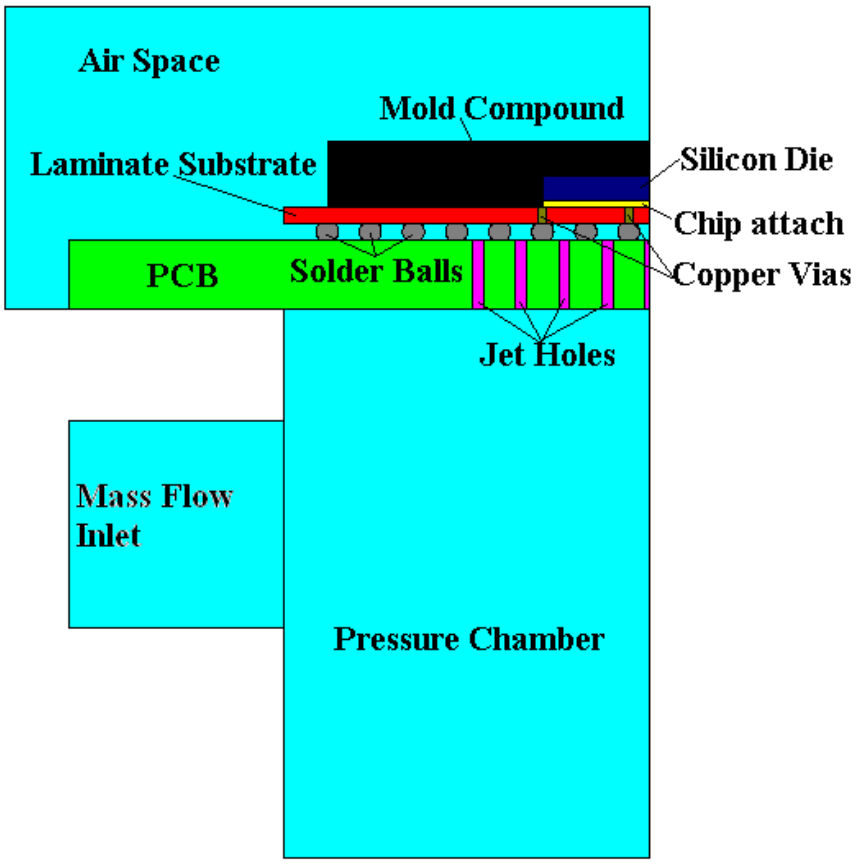


Figure V.1: The numerical model geometry.

A mesh size study was performed on all four numerical models to ensure accurate results. Approximate material properties were used for the mesh study. The same boundary conditions and heat loads were used with each of the different mesh sizes. Each model was run with first order accuracy and a convergence criterion of 0.001 for the continuity and momentum equations and 0.000001 for the energy. Once the convergence

criterion was met the maximum temperature and fluid velocity was compared among the mesh sizes. The results are shown in the table V.1 below.

Table V.1: Mesh size study for the four jet hole geometry numerical models.

# of Nodes	135269	142487	162549	135269	142487	162549
	Temperature (K)			Velocity (m/s)		
0.250 mm Centered	398.5677	398.9904	398.7844	30.896	31.07622	31.2574
# of Nodes	199209	201554	239284	199209	201554	239284
	Temperature (K)			Velocity (m/s)		
0.250 mm X	402.8879	402.9487	403.0906	39.808	40.01718	39.93946
# of Nodes	275806	287968	302548	275806	287968	302548
	Temperature (K)			Velocity (m/s)		
0.368 mm Centered	396.658	398.3966	396.9094	10.34825	10.28254	10.34344
# of Nodes	202758	218251	240371	202758	218251	240371
	Temperature (K)			Velocity (m/s)		
0.368 mm X	402.3325	402.5543	402.9606	15.85399	16.33907	16.06094

As the number of nodes in the mesh increased, both the maximum velocity and temperature stayed relatively close to one another. Both the temperature and the velocity stayed within 0.5 K and 0.5 m/s of each other respectively. The more the nodes the longer the computational time required for each model. So, the middle mesh size for each model was selected for the numerical analysis.

The material properties for the PBGA used in the experiments were different then the ones used in the initial modeling. This was due to modifications performed on the PBGA in order to contain the resistive heater and thermocouple within the mold compound. Also the laminate substrate consisted of more copper layers which made it

more thermally conductive then the in initial model. The PCB contained the copper leads to create Joule heating in the interconnects, which increased its thermal conductivity. The material properties used in the four jet hole geometry models are described in Table V.2.

Table V.2: Material properties used in the numerical models of the four jet hole geometries.

Materials	Density	Specific Heat	Thermal Conductivity	Viscosity	Molecular Weight	Heat Load
	kg/m^3	J/kgK	W/mK	kg/ms	kg/kgmol	W
Air	1.225	1006.43	0.0242	1.7894×10^{-5}	28.966	NA
Mold Compound	1900	905	1	NA	NA	NA
Silicon Chip	1685	712	130	NA	NA	1, 2, 3
Chip Attach	3500	500	2	NA	NA	NA
Copper Vias	8978	381	387.6	NA	NA	NA
Laminate Substrate	2000	547	6	NA	NA	NA
Solder Balls	8340	150	50.1	NA	NA	0.4, 1
PCB	1978	289	3	NA	NA	NA

Model Validation

The numerical models included natural convection heat transfer. As the package increased in temperature this parameter became more significant. Natural convection was based on the Boussinesq approximation, which assumes constant fluid density with the exception of the buoyancy term in the momentum equation. Radiation was neglected

in the models because of the low temperature ranges measured in the experiments and also based on an analytical calculation for the radiative exchange between the PBGA and the PCB directly under it. These two surfaces were chosen because they constituted the largest surface areas for radiative exchange.

Both the bottom of the PBGA and the PCB were considered to be gray and diffuse surfaces. The solder balls were excluded because they greatly increased the complexity of the analytical calculation. The two surfaces were assumed to form an enclosure so that they exchanged radiation only with each other. The equation used to estimate the heat transfer between the two surfaces due to radiation was

$$q_{12} = \frac{A\sigma(T_1^4 - T_2^4)}{\frac{1}{\varepsilon_1} + \frac{1}{\varepsilon_2} - 1} \qquad \text{(V.1)}$$

where A was the surface area of both the bottom of the PBGA and the PCB, T_1 was the average temperature of the bottom of the PBGA, T_2 was the average temperature of the PCB, ε_1 and ε_2 were the emissivities of the bottom of the PBGA and PCB respectively, and σ was the Stefan-Boltzmann constant. Equation V.1 was derived using the resistive network method under the assumptions of two diffuse and gray infinite surfaces that form an enclosure. The surfaces were assumed to be infinitely large due to the ratio between the length of the surfaces and the distance between them.

The average temperature at the bottom of the PBGA when a 3 W of power was supplied to the chip was 368 K for the 0.250 mm centered jet hole pattern. The average temperature of the PCB directly under the PBGA when a 3 W of power was supplied to the chip was 363 K for the 0.250 mm centered jet hole pattern. The areas of the two surfaces were assumed to be the same and were equal to 0.000289 m^2. The emissivity of

both the bottom of the PBGA and the PCB were assumed to be 0.8 because they consisted mostly of FR4 material [Shidore, 2000]. All of these values were inserted into equation V.1 and the total heat transfer rate due to radiation was calculated to be 0.011 W. This was only 0.4% of the total heat generated, thus radiation was excluded from the models.

An extensive numerical analysis was performed on the 0.250 mm centered jet hole design to ensure that the geometry, material properties, and boundary conditions were accurate. All the experiments performed on the 0.250 mm centered pattern were conducted numerically. The models were assumed laminar based on the analytical Reynolds number calculations in Appendix A which were well below the laminar region for internal flow. All the models were run to steady state. A mass flow rate of 9.45×10^{-6} kg/s was used as the inlet boundary condition depicted in figure V.1 for this particular geometry which was based on the average flow rate measurements from the experiments. Several of the models included top level fan cooling, as was also performed in the experiments. The assumed air velocity for top level fan cooling used in the numerical models was 1 m/s. The model gave insights on the complete temperature profile, jet exit velocities, heat transfer coefficients, and many other parameters that the experiments did not give. Table V.3 shows a temperature comparison between the numerical and experimental results for the 0.250 mm centered design.

Table V.3: A temperature comparison between the numerical and experimental results for the 0.250mm centered jet hole design.

Chip level heat load (W)	Solder ball heat load (W)	IC	Fan	Experimental Chip Level Temperature (K)	Numerical Chip Level Temperature (K)	%	Experimental Avg. Solder Ball Temperature (K)	Numerical Avg. Solder Ball Temperature (K)	%
1	0.4	X		331	335	1.3	312	321	3.0
1	0.4		X	341	340	0.4	325	325	0.2
2	0.4	X		361	366	1.5	323	340	5.2
2	0.4		X	380	379	0.4	346	346	0.1
3	0.4	X		395	397	0.5	336	356	5.9
3	0.4		X	419	416	0.7	365	369	1.3
3	0.4	X	X	378	381	0.8	325	345	6.2
0	1	X		304	311	2.4	304	311	2.3
0	1		X	311	314	1.0	311	313	0.4

The model predicted chip level temperatures better then it predicted the solder ball temperatures. This was due to several factors including; the error inherent in the instruments used in the experiments, the approximate material properties used in the model, the location of the thermocouples in the solder balls, and the perfect symmetry of the model. Another contribution to the difference between the experimental and numerical result was in the jet hole diameters. The hole diameters used in the model were based off the nominal drill diameters of 0.250 mm and 0.368 mm, where as the experimental jet holes were closer to 0.32 mm and 0.40 mm. The maximum chip level and solder ball temperature difference between the experimental and numerical results was when both interconnect cooling and fan cooling were used with 3 W chip level and 0.4 W solder ball heat loads. All of the temperatures from the numerical results were within 6.2% of the experimental results. The equation used to calculate this temperature percentage was

$$\% = \frac{T_{numerical} - T_{experimental}}{T_{experimental}} X 100 \qquad \text{(V.2)}$$

where $T_{numerical}$ was the model predicted temperature and $T_{experimental}$ was the measured experimental temperature. Thus, the numerical results captured the fundamental trends of experimental data.

Since the modeling and experimental results were close, three other models were developed based on the other jet hole designs. The same material properties used in the 0.250 mm centered jet hole design were used in the other three models. Using the same properties for all four models allowed a direct comparison between each of the jet hole designs. Table V.3 shows the material properties used in the four numerical models of the jet hole geometries.

Comparisons between the Four Jet Hole Design Models

The 1 W, 2 W, and 3 W chip level heat loads with a 0.4 W solder ball heat load were compared through numerical modeling. The PBGA, PCB, and air space were exactly the same between the models with the exception of the jet hole diameters and patterns. The material properties shown in Table V.2 were used in all of the four model geometries. The mass flow rate boundary conditions were based upon the flow rate measurements of the four jet hole designs. The chip level and average solder ball temperatures, maximum jet velocity, and average heat transfer coefficients at various locations were compared among the models. Table V.4 shows results for the four numerical models with only direct interconnect cooling.

Table V.4: The temperatures at various locations, heat transfer coefficients, and maximum jet hole velocities from the four jet hole design models at various chip level heat loads.

Model				Model			
0.250 mm Centered	Mass flow Inlet	(kg/s)	9.45×10^{-6}	0.368 mm Centered	Mass flow Inlet	(kg/s)	9.63×10^{-6}
Chip level heat load	1 W	2 W	3 W	Chip level heat load	1 W	2 W	3 W
Chip Level Temperature (K)	335	366	397	Chip Level Temperature (K)	334	365	395
Avg. Solder Ball Temperature (K)	321	340	356	Avg. Solder Ball Temperature (K)	321	341	355
Avg. Top PBGA Surface h (W/m^2K)	29	32	34	Avg. Top PBGA Surface h (W/m^2K)	26	27	27
Avg. Solder ball and bottom PBGA Surface h (W/m^2K)	119	139	148	Avg. Solder ball and bottom PBGA Surface h (W/m^2K)	115	133	141
Maximum Jet Hole Velocity (m/s)	29	29	29	Maximum Jet Hole Velocity (m/s)	10	10	10
0.250 mm X	Mass flow Inlet	(kg/s)	9.41×10^{-6}	0.368 mm X	Mass flow Inlet	(kg/s)	9.32×10^{-6}
Chip level heat load	1 W	2 W	3 W	Chip level heat load	1 W	2 W	3 W
Chip Level Temperature (K)	336	369	401	Chip Level Temperature (K)	337	370	403
Avg. Solder Ball Temperature (K)	322	342	361	Avg. Solder Ball Temperature (K)	322	342	362
Avg. Top PBGA Surface h (W/m^2K)	24	26	28	Avg. Top PBGA Surface h (W/m^2K)	17	18	30
Avg. Solder ball and bottom PBGA Surface h (W/m^2K)	136	141	150	Avg. Solder ball and bottom PBGA Surface h (W/m^2K)	118	125	133
Maximum Jet Hole Velocity (m/s)	38	38	38	Maximum Jet Hole Velocity (m/s)	15	15	15

The solder ball temperatures were found by taking the average between the center and outer solder balls. The same method was used to obtain the average heat transfer coefficients for both the bottom and top of the PBGA package. The maximum jet hole velocity was found within the jets themselves. This value does not represent the impact velocity at the bottom of the PBGA package. Figure V.2 shows the isometric view temperature profile of 0.250 mm centered pattern with interconnect cooling of a 3 W chip level and 0.4 W solder ball heat load.

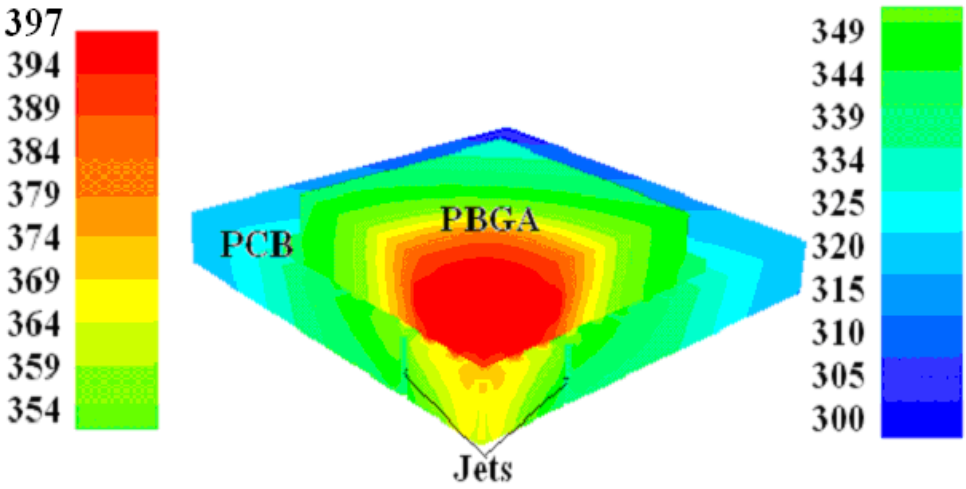


Figure V.2: A top isometric view of the temperature (K) profile for the PBGA package.

The most effective design for cooling the chip was the 0.368 mm centered pattern which had a 1.9 K improvement over the next best 0.250 mm centered design. The centered patterns concentrated the air flow directly below the chip, thus it cooled it more effectively. The 0.250 mm and 0.368 mm centered patterns were also more successful in cooling the solder balls. The X pattern jet holes did not focus the cooling on the center of the PBGA, which had the highest temperature ranges. This resulted in a higher overall

temperature profile. The X jet hole design did cool the peripheral solder balls better then the centered pattern, which will be come more important as Joule heating increases in the interconnects. Figure V.3 shows the bottom of the PBGA package temperature profile for both the 0.250 mm and 0.368 centered patterns. Figure V.4 shows the bottom of the PBGA package temperature profile for both the 0.250 mm and 0.368 X patterns. All four models were run with a 3 W chip level and 0.4 W solder ball heat load.

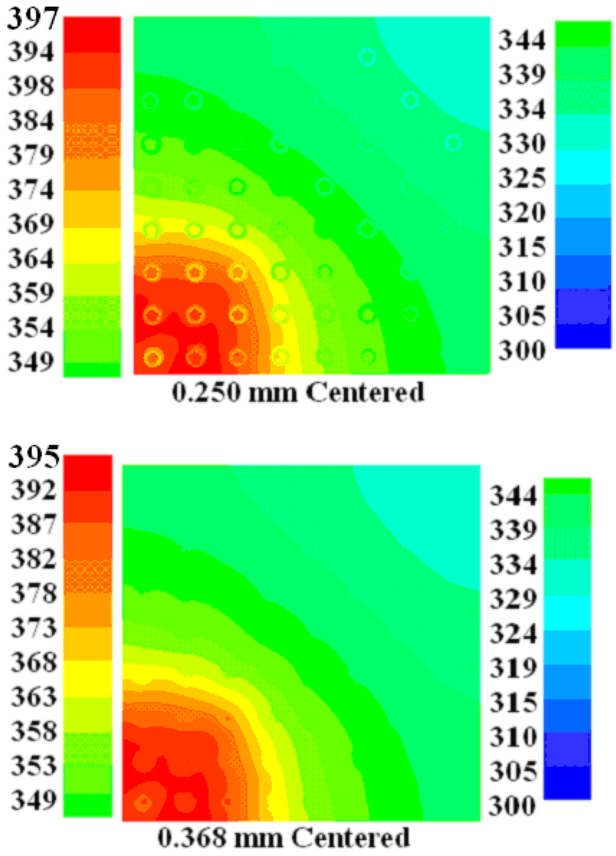


Figure V.3: The temperature (K) profile of the solder ball and bottom of the PBGA package with the centered interconnect cooling design.

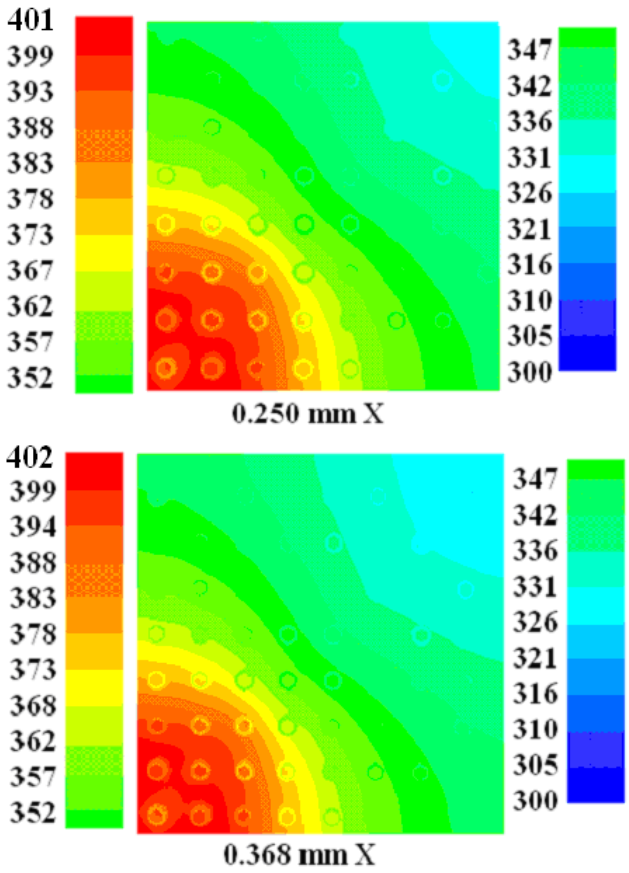


Figure V.4: The temperature (K) profile of the solder balls and bottom of the PBGA package with the X interconnect cooling design.

PBGA Heat Path Analysis

Another critical parameter acquired from the model, was how the heat moved through the PBGA package based on the thermal management schemes. The heat transfer coefficients and temperatures in Table V.4 were used to calculate the amount of heat leaving from the top and bottom of the PBGA package. The equation used to obtain the heat transfer rate was

$$q = h \cdot A \cdot (T_{avg.} - T_{bulk}) \qquad \text{(V.3)}$$

where h was the heat transfer coefficient calculated by the model, A was the surface area, $T_{avg.}$ was the average temperature of the PBGA, and T_{bulk} was the average between the air and PBGA temperatures. The amount of heat calculated for the two locations were compared to the overall heat load and was converted into a percentage. Figure V.5 shows the heat percentage leaving the bottom and top of the PBGA package for a 3 W chip level and 0.4 W solder ball heat load.

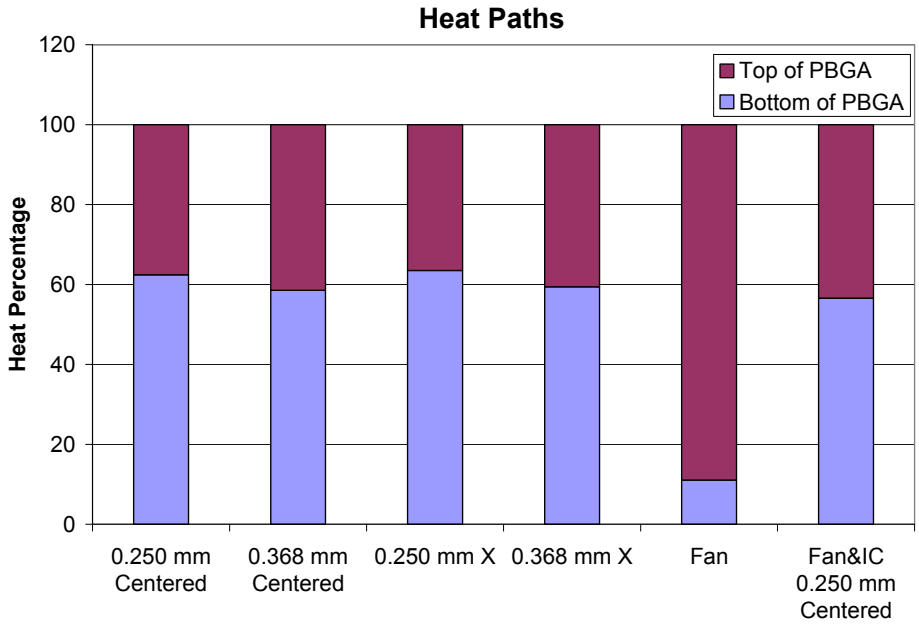


Figure V.5: The percentage of heat leaving the bottom and top of the PBGA package.

Most of the heat travels through the bottom of the package when only direct interconnect cooling was used. The 0.368 mm X was the most effective for cooling the entire bottom surface and solder balls of the PBGA package, so most of the heat generated in the chip transferred through the bottom. When only the top level fan cooling was used, most of the heat transferred through the top of the package; however, the chip level and solder ball temperatures were much higher then in the other cases. In the case

where both top level and interconnect cooling were used, the majority of the heat transferred through the bottom of the PBGA package. However, a significant amount of heat transferred through the top of the package. This heat percentage analysis showed that a significant amount of the heat generated in an IC transfers through the bottom of the package.

The modeling allowed a more comprehensive study of direct interconnect cooling. It showed the effectiveness of each jet hole design based on the same PBGA geometry, materials, and heat loads. This ability allowed the designs to be compared directly with each other, so that best jet hole diameter and pattern could be determined. The most effective jet hole design for cooling both the solder balls and chip was the centered pattern. The centered pattern concentrated most of the cooling in the center of the PBGA where most of the heat was located. This reduced the temperature profile through out the package. The X pattern may not have been as effective in cooling PBGA package, but did cool the periphery sold balls better then the centered pattern.

The experimental data was difficult to compare with the numerical modeling because of the inconsistency of the PBGA test packages used in the experiments. If all of the experiments could have been done with a single PBGA package, the results from all of the four jet hole designs would be comparable to the model. The modeling and experimental results did show that the center pattern was more effective in reducing the chip level and average solder ball temperatures. They also show that direct interconnect cooling was more effective then the top level fan cooling for all heat loads. Both the modeling and experimental results show that possibly using a combination of centered and periphery jet holes will be the most effective cooling solution

CHAPTER VI

CONCLUSION AND RECOMMENDATIONS

Removing heat from packaged chips is difficult due to the internal thermal resistance. Dense BGA interconnects provide a thermally conductive path to the chip through thermal vias and electrical leads, which can be utilized for cooling. The initial PBGA modeling illustrated the effects of cooling the solder balls of packaged chips. The maximum temperature was decreased by 50 K over the baseline model. This drastic reduction in temperature will greatly increase the reliability of the electronic chip and will increase its operational lifetime.

To verify if cooling the solder balls and underside of the chip was effective, four jet hole geometries where incorporated into a PCB. Centered and X patterns with 0.250 mm and 0.368 mm diameter jet holes were used in the experiments. The PCB also contained the necessary leads to simulate Joule heating in the solder balls of a daisy-chained PBGA package. A resistive heater was embedded into the PBGA package to simulate chip level heating. Five thermocouples were incorporated into various solder balls during the reflow process so that their temperature could be monitored during the experimentation. Two compressors were used to provide the necessary air pressure

required for jet impingement cooling. The flow rate and pressure were monitored and recorded for each experiment.

A number of experimental variations on the four jet hole designs tested different aspects of interconnect cooling. Direct interconnect cooling was compared to top level fan cooling at a given chip level and solder ball heat load. Next, interconnect and fan cooling were compared with only solder ball heating. Multiple experiments were done with the same parameters to ensure that the data were repeatable. The results from the 0.250 mm centered pattern were looked at extensively showing significant cooling over top level fan cooling. The other jet hole geometries were then compared with each other.

Since each of the four jet hole patterns had a different PBGA package with a unique heater, thermocouple, and silicon die location the temperature measurements between designs could not be compared directly. However, the temperature difference between interconnect cooling and top level cooling for each experimental jet hole design were compared. The flow rate and pressure sensor measurements could be directly compared between the jet hole designs because the same instruments were used for each experiment. The experimental results showed that the 0.250 mm centered jet hole pattern was the most effective in cooling both the chip and solder balls. The chip temperature was reduced by 23 K over top level fan cooling for a 3 W chip level and 0.4 W heat load. The solder balls were cooled an average of 27 K over top level fan cooling with a 3 W chip level and 0.4 W solder ball heat load.

Once all of the experiments were completed the flow rate and pressure measurements were used as boundary conditions in the numerical models. They also gave detailed information about the physics of direct interconnect cooling that the

experiments could not. A model of the 0.250 mm centered design was adjusted so that it matched the experimental results. Once they were close, three other models were constructed representing the three other jet hole designs. All four models had the same PBGA architecture and material properties which allowed them to be compared directly.

The model results showed the centered pattern jet holes cooled both the solder balls and chip more effectively then did the X design. The X pattern did cool the peripheral solder balls better then the centered pattern. The models gave insight on average heat transfer coefficients on the bottom and top of the package. This aided in predicting how the heat moved through the PBGA package. Most of the heat generated by the chip transferred through the bottom of the PBGA in all thermal management scenarios with the exception of just top level fan cooling. The numerical modeling provided a significantly greater amount of information about the physics behind the direct interconnect cooling then did the experiments.

The experimental results for each jet hole design were hard to compare, because of the differences between each PBGA test chip. They did however show that direct interconnect cooling was practical and useful for cooling packaged ICs. The modeling showed what jet hole design was the most effective. Based upon the results of the model, using a combination of centered and peripheral jet holes is ideal for maximizing heat rejection away from the interconnects and chip.

Jet impingement on the bottom side of the package has been shown to effectively cool the solder balls and chip of a PBGA package. Future experiments should focus on different jet hole diameters and geometries. The flow rate is the key to providing excellent cooling. The higher the flow rate the better the cooling, however, the pressure

drop through the jets increase. Compressors come in all shapes and sizes with different characteristics. Investigation into a compact high flow rate compressor would be worth studying for future experiments. Finally, direct interconnect cooling of different electronic packages should be investigated.

Jet impingement is one solution to cooling the off-chip metal interconnects. Eventually, air will not be able to effectively cool future packaged chips because of its limited heat transfer properties. Possibly using a dielectric fluid may be implemented instead of air to increase heat transfer. Whether liquid or air is used as the heat transfer fluid, directly cooling the interconnects has been shown through modeling and experimentation to be an effective solution for reducing the temperatures in packaged chip architectures.

APPENDIX A

PRESSURE DROP AND FLOW RATE CALCULATIONS

Hargraves BTC Diaphragm Compressor

Pump Pressure (Pa)	Pump Pressure (psi)	Flow Rate (m^3/s)	Flow Rate (lpm)	Exit Velocity (m/s)	f	Re	hf	Pressure Drop (Pa)	Pressure Drop (psi)	Pressure Difference (Pa)	Pressure (psi)
0.00	0.00	5.00E-05	3.00	36.38	3.76	572.35	711.05	8,869.73	1.3308	-8,869.73	-1.33079
5000.00	0.73	4.57E-05	2.74	33.23	3.79	522.81	597.28	7,446.29	1.1172	-2,446.29	-0.36703
10000.00	1.45	4.17E-05	2.50	30.32	3.82	477.11	501.13	6,243.60	0.9368	3,756.40	0.56360
15000.00	2.18	3.80E-05	2.28	27.65	3.85	435.07	420.15	5,231.00	0.7848	9,769.00	1.46571
20000.00	2.90	3.46E-05	2.08	25.20	3.89	396.52	352.18	4,381.41	0.6574	15,618.59	2.34337
25000.00	3.63	3.16E-05	1.89	22.96	3.92	361.29	295.33	3,671.01	0.5508	21,328.99	3.20014
30000.00	4.35	2.88E-05	1.73	20.92	3.97	329.21	247.93	3,078.96	0.4620	26,921.04	4.03915
35000.00	5.08	2.62E-05	1.57	19.07	4.02	300.11	208.52	2,587.08	0.3882	32,412.92	4.86314
40000.00	5.80	2.39E-05	1.44	17.40	4.07	273.81	175.87	2,179.63	0.3270	37,820.37	5.67445
45000.00	6.53	2.19E-05	1.31	15.90	4.13	250.14	148.88	1,843.04	0.2765	43,156.96	6.47514
50000.00	7.25	2.00E-05	1.20	14.55	4.19	228.94	126.62	1,565.64	0.2349	48,434.36	7.26695
55000.00	7.98	1.83E-05	1.10	13.35	4.26	210.02	108.31	1,337.51	0.2007	53,662.49	8.05136
60000.00	8.70	1.69E-05	1.01	12.28	4.33	193.22	93.26	1,150.18	0.1726	58,849.82	8.82965
65000.00	9.43	1.56E-05	0.93	11.34	4.41	178.37	80.91	996.53	0.1495	64,003.47	9.60289
70000.00	10.15	1.44E-05	0.87	10.51	4.49	165.29	70.78	870.55	0.1306	69,129.45	10.37197
75000.00	10.88	1.34E-05	0.81	9.78	4.58	153.82	62.47	767.20	0.1151	74,232.80	11.13767
80000.00	11.60	1.26E-05	0.75	9.14	4.67	143.77	55.63	682.27	0.1024	79,317.73	11.90059
85000.00	12.33	1.18E-05	0.71	8.58	4.76	134.99	49.98	612.21	0.0919	84,387.79	12.66129
90000.00	13.05	1.11E-05	0.67	8.09	4.85	127.29	45.30	554.08	0.0831	89,445.92	13.42020
95000.00	13.78	1.05E-05	0.63	7.66	4.94	120.51	41.37	505.40	0.0758	94,494.60	14.17769
100000.00	14.50	1.00E-05	0.60	7.28	5.03	114.47	38.03	464.05	0.0696	99,535.95	14.93408
105000.00	15.23	9.52E-06	0.57	6.93	5.13	109.00	35.14	428.24	0.0643	104,571.76	15.68963
110000.00	15.95	9.08E-06	0.54	6.61	5.23	103.94	32.57	396.44	0.0595	109,603.56	16.44459
115000.00	16.95	8.66E-06	0.52	6.30	5.34	99.10	30.22	367.33	0.0551	129,632.67	19.44970
120000.00	17.95	8.24E-06	0.49	6.00	5.46	94.32	27.99	339.77	0.0510	134,660.23	20.20402
125000.00	18.95	7.81E-06	0.47	5.68	5.60	89.43	25.81	312.79	0.0469	139,687.21	20.95825
130000.00	19.95	7.36E-06	0.44	5.35	5.77	84.25	23.61	285.61	0.0429	144,714.39	21.71251
135000.00	20.95	6.87E-06	0.41	5.00	5.99	78.61	21.34	257.67	0.0387	149,742.33	22.46689
140000.00	21.95	6.32E-06	0.38	4.60	6.29	72.34	18.99	228.65	0.0343	-228.65	-0.03431
145000.00	22.95	5.70E-06	0.34	4.15	6.74	65.28	16.55	198.55	0.0298	-198.55	-0.02979
150000.00	23.95	5.00E-06	0.30	3.64	7.44	57.23	14.06	167.88	0.0252	-167.88	-0.02519

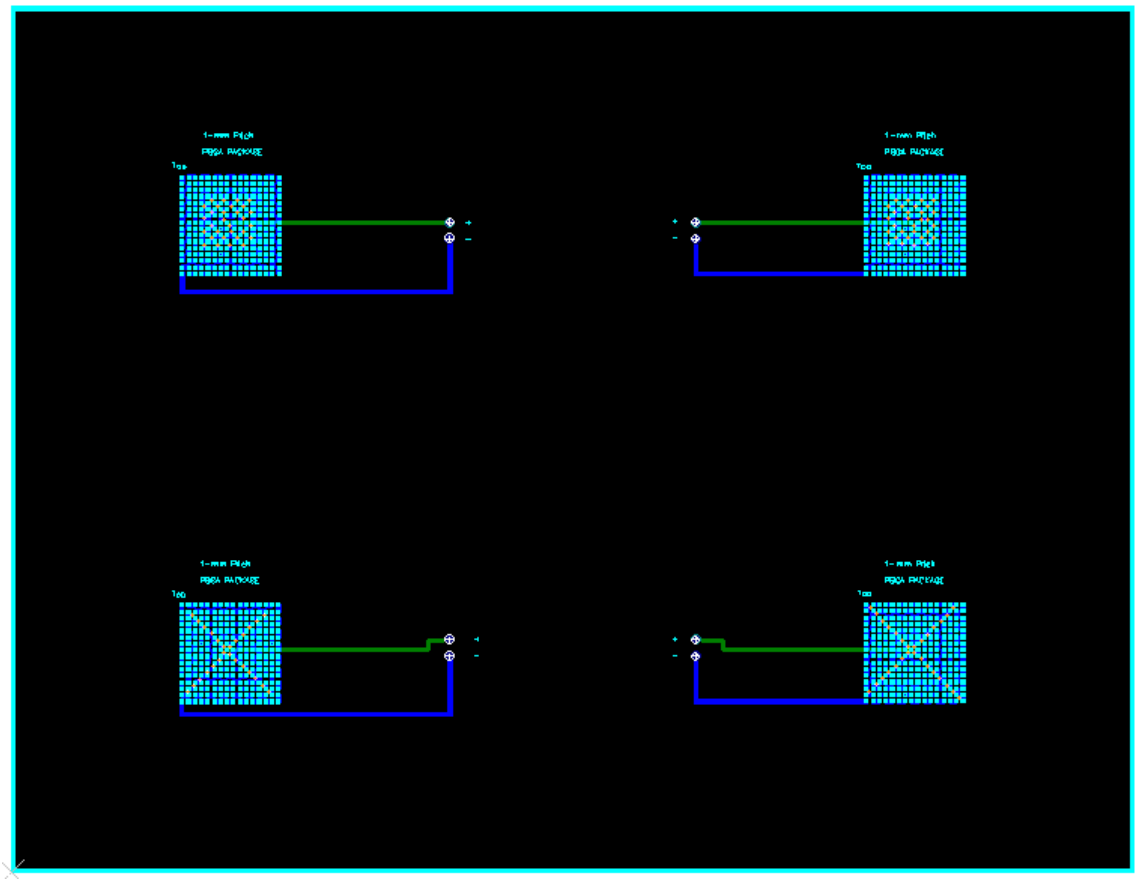
Thomas Rietschle Rotary Compressor

Pump Pressure (Pa)	Pump Pressure (psi)	Flow Rate (m^3/s)	Flow Rate (lpm)	Exit Velocity (m/s)	f	Re	hf	Pressure (Pa)	Pressure Difference (Pa)	psi pressure drop	lpm flow rate
0.00E+00	0	3.34E-04	20.07	234.93	3.55	3.70E+03	27941.7928	3.50E+05	-3.50E+05	52.57	-2.14E+04
1.38E+03	0.2	3.27E-04	19.60	229.53	3.55	3.61E+03	26680.1491	3.35E+05	-3.33E+05	50.20	-1.86E+04
2.76E+03	0.4	3.20E-04	19.19	224.67	3.55	3.53E+03	25567.3123	3.21E+05	-3.18E+05	48.10	-1.63E+04
4.14E+03	0.6	3.14E-04	18.81	220.24	3.55	3.47E+03	24575.6632	3.08E+05	-3.04E+05	46.24	-1.44E+04
5.52E+03	0.8	3.08E-04	18.46	216.17	3.55	3.40E+03	23679.839	2.97E+05	-2.91E+05	44.55	-1.29E+04
6.89E+03	1	3.02E-04	18.14	212.35	3.55	3.34E+03	22856.3792	2.87E+05	-2.80E+05	43.00	-1.15E+04
8.27E+03	1.2	2.97E-04	17.83	208.71	3.55	3.28E+03	22083.4509	2.77E+05	-2.69E+05	41.55	-1.04E+04
9.65E+03	1.4	2.92E-04	17.52	205.15	3.55	3.23E+03	21340.6557	2.68E+05	-2.58E+05	40.15	-9.33E+03
1.10E+04	1.6	2.87E-04	17.22	201.58	3.55	3.17E+03	20608.916	2.58E+05	-2.47E+05	38.77	-8.37E+03
1.24E+04	1.8	2.82E-04	16.90	197.91	3.55	3.11E+03	19870.4426	2.49E+05	-2.37E+05	37.38	-7.47E+03
1.38E+04	2	2.76E-04	16.57	194.05	3.56	3.05E+03	19108.7815	2.40E+05	-2.26E+05	35.95	-6.62E+03
1.52E+04	2.2	2.70E-04	16.22	189.92	3.56	2.99E+03	18308.9425	2.30E+05	-2.14E+05	34.44	-5.79E+03
1.65E+04	2.4	2.64E-04	15.84	185.42	3.56	2.92E+03	17457.6071	2.19E+05	-2.02E+05	32.84	-4.99E+03
1.79E+04	2.6	2.57E-04	15.41	180.47	3.56	2.84E+03	16543.4168	2.07E+05	-1.89E+05	31.12	-4.22E+03
1.93E+04	2.8	2.49E-04	14.94	174.97	3.56	2.75E+03	15557.343	1.95E+05	-1.76E+05	29.26	-3.48E+03
2.07E+04	3	2.40E-04	14.42	168.84	3.56	2.66E+03	14493.1353	1.82E+05	-1.61E+05	27.26	-2.78E+03
2.21E+04	3.2	2.31E-04	13.83	161.98	3.56	2.55E+03	13347.8523	1.67E+05	-1.45E+05	25.10	-2.15E+03
2.34E+04	3.4	2.20E-04	13.18	154.30	3.57	2.43E+03	12122.4711	1.52E+05	-1.28E+05	22.80	-1.58E+03
2.48E+04	3.6	2.07E-04	12.45	145.72	3.57	2.29E+03	10822.5781	1.36E+05	-1.11E+05	20.35	-1.10E+03
2.62E+04	3.8	1.94E-04	11.63	136.15	3.58	2.14E+03	9459.13987	1.19E+05	-9.23E+04	17.78	-7.11E+02
2.76E+04	4	1.79E-04	10.72	125.50	3.58	1.97E+03	8049.3545	1.01E+05	-7.33E+04	15.13	-4.18E+02
2.90E+04	4.2	1.62E-04	9.71	113.67	3.59	1.79E+03	6617.58336	8.29E+04	-5.39E+04	12.44	-2.15E+02
3.03E+04	4.4	1.43E-04	8.59	100.58	3.60	1.58E+03	5196.36313	6.51E+04	-3.47E+04	9.76	-8.90E+01
3.17E+04	4.6	1.23E-04	7.36	86.14	3.61	1.36E+03	3827.49847	4.79E+04	-1.62E+04	7.19	-2.25E+01
3.31E+04	4.8	1.00E-04	6.00	70.25	3.64	1.11E+03	2563.23513	3.21E+04	1.02E+03	4.81	5.92E+00
3.45E+04	5	7.52E-05	4.51	52.84	3.68	8.31E+02	1467.51431	1.83E+04	1.61E+04	2.75	1.51E+01

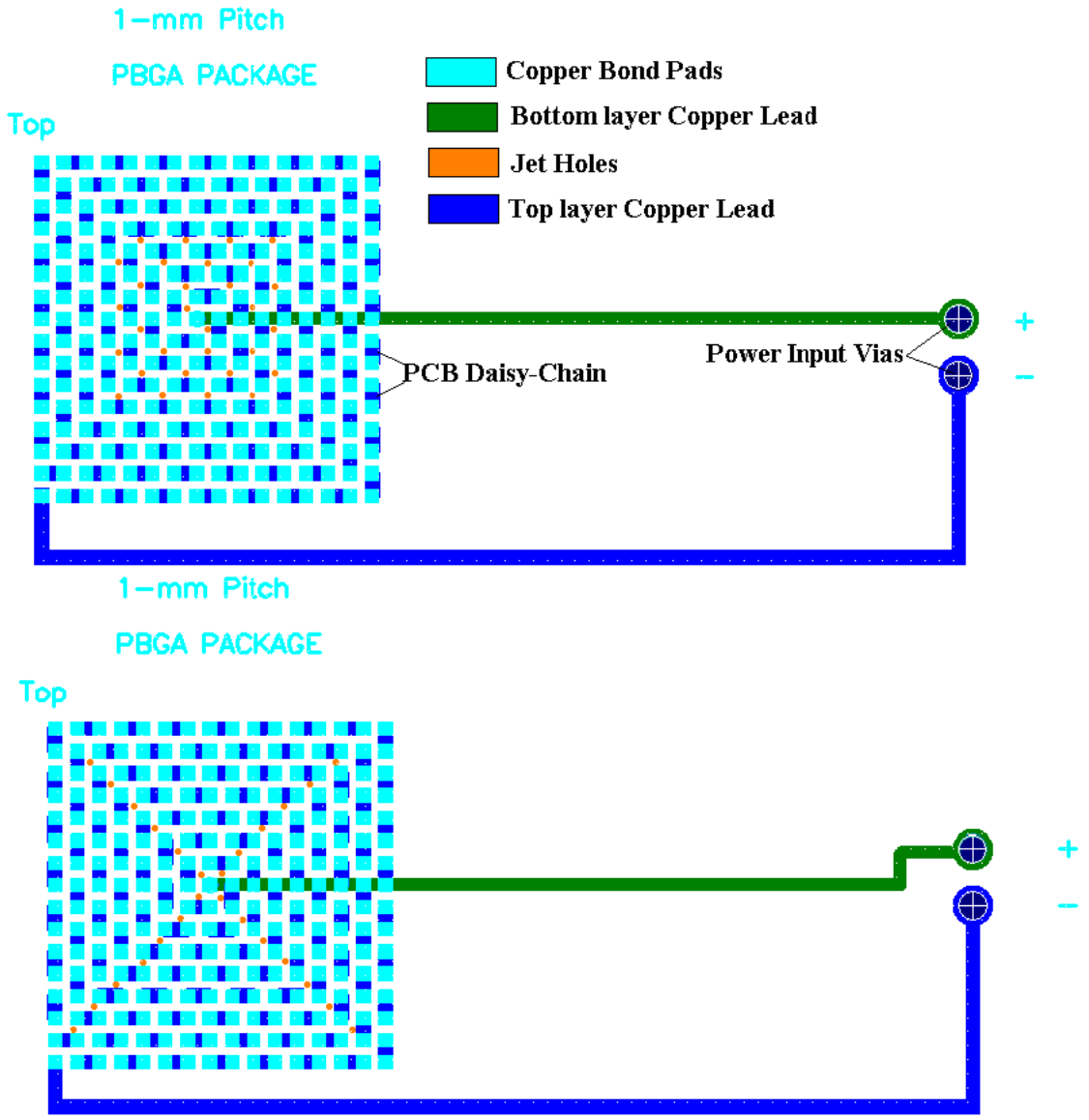
APPENDIX B

EXPERIMENTAL DESIGNS

PCB Design Layout



Individual PCB Designs



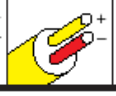
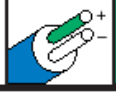
Jet Hole Diameters

	0.368 mm Drill Size	0.250 mm Drill Size
1	0.399	0.347
2	0.398	0.341
3	0.400	0.331
4	0.404	0.337
5	0.402	0.335
6	0.433	0.331
7	0.391	0.310
8	0.401	0.311
9	0.395	0.316
10	0.402	0.324

APPENDIX C

EQUIPMENT SPECIFICATIONS

Special Limits K-Type Thermocouples

ANSI Code	ANSI MC 96.1 Color Coding: Thermocouple Grade	ANSI MC 96.1 Color Coding: Extension Grade	Alloy Combination: + Lead	Alloy Combination: – Lead	Comments Environment Bare Wire	Maximum T/C Grade Temp. Range	EMF (mV) Over Max. Temp. Range	IEC 584-3 Color Coding: Thermocouple Grade	IEC 584-3 Color Coding: Intrinsically Safe	IEC Code
K			CHROMEGA® NICKEL-CHROMIUM Ni-Cr	ALOMEGA® NICKEL-ALUMINUM Ni-Al (magnetic)	Clean Oxidizing and Inert. Limited Use in Vacuum or Reducing. Wide Temperature Range, Most Popular Calibration	–270 to 1372°C –454 to 2501°F	–6.458 to 54.886			K

K	Temp Range	>0 to 1250°C	>32 to 2282°F	0 to 1250°C	32 to 2282°F
	Tolerance Value	2.2°C or 0.75%	4.0°F or 0.75%	1.1°C or 0.4%	2.0°F or 0.4%
	Temp. Range*	-200 to 0°C	-328 to 32°F		
	Tolerance Value	2.2°C or 2.0%	4.0°F or 2.0%		

Fathom Flow Meter

Features	Applications
• Thermal Sensor • 1% Accuracy w/ 100:1 turndown ratio • Integral Valve, Display & Setpoint • Linear Output (0-5 VDC, 4-20 ma) • Single ended power supply • Delrin, Optional 316 Stainless Flow Body • NIST Traceable Calibration • Low Cost	• OEM • Laboratory • Medical • Process Control • Pharmaceutical • Leak Detection • R & D • Gas Blending

Wika Pressure Transducer

Wika Model:	8415072 Type S-10
Input Pressure:	0-5 PSI
Pressure Connection:	1/2" NPT male
Electrical Output:	4-20 mA 2-wire
Excitation:	10-30 VDC power supply
Electrical Load Limit:	Resistance=(supply voltage-10 V)/0.02 A
Maximum Pressure:	30 PSI
Burst Pressure:	30 PSI
Accuracy:	0.25% of span BFSL (Hysteresis 0.1%, Repeatability 0.05%)
Response Time:	1 ms
Temperature Range:	Media -25 °F to 212 °F, Ambient -5 °F to 175 °F
Temp Compensated:	32 °F to 175 °F
Electrical Connection:	DIN 43650 Plug Connector (IP65/NEMA 5) with solderless screw terminal
Electrical Protection:	Protected against reverse polarity, short circuit and overvoltage
Transmitting Liquid:	Silicone oil
Wetted Parts:	316 stainless steel (parts in contact with media)
Case Material:	304 Stainless Steel

Agilent E3620A Power Supply

Specifications

	E3610A	E3611A	E3612A	E3614A	E3615A	E3616A	E3617A	E3620A	E3630A
Features	Dual range, 10 turn pots, Constant Voltage (CV), Constant Current (CC) modes.			Adjustable overvoltage protection, voltage & resistance programming, remote sense, rear outputs, ten turn pots, CV, CC modes. Multiple supplies can be connected for tracking or higher power.				Isolated dual outputs, 10 turn pots CV, CL	Tracking, CV, CL (±20 V) CV, CF (+6 V)
Number of outputs	1							2	3
Number of output Ranges	2	2	2	1	1	1	1	1	1
dc Output Rating	8 V, 3 A 15 V, 2 A	20 V, 1.5 A 35 V, 0.85 A	60 V, 0.5 A 120 V, 0.25 A	8 V, 6 A	20 V, 3 A	35 V, 1.7 A	60 V, 1 A	25 V, 1 A 25 V, 1 A	+6 V, 2.5 A +20 V, 0.5 A -20 V, 0.5 A
Load and Line Regulation	<0.01% + 2 mV								
Ripple and Noise (20 Hz to 20 MHz)									
Normal mode voltage	<200 µVrms, <2 mVpp			<200 µVrms, <1 mVpp				<350 µVrms, <1.5 mVpp	
Normal mode current	<200 µVrms / 1 mApp			<0.02%+ 3 mA	<0.02%+ 1.5 mA	<0.02%+ 1 mA	<0.02%+ 0.5 mA	–	
Common mode current	not specified							<1 µArms	
Transient Response Time:	<50 µsec following change in output current from full load to half load for output to recover to within:								
	10 mV			15 mV					
Meter Accuracy	±0.5% + 2 counts at 25°C ±5°C								
Meter Resolution									
Voltage	10 mV	100 mV	100 mV	10 mV	10 mV (0-20 V), 100 mV (>20 V)				10 mA
Current	10 mA	10 mA	1 mA	10 mA	10 mA	1 mA	1 mA	1 mA	10 mA
Isolation	240 Vdc								

Supplemental Characteristics

Control Mode	CV/CC							CV/CL	CV/CL (±20 V) CV/CF (+6 V)
Temperature Coefficient per °C									
Voltage	<0.02% + 1 mV			<0.02% + 500 µV				<0.02% + 1 mV	
Current	<0.02% + 2 mA			<0.02% + 3 mA	<0.02% + 1.5 mA	<0.02% + 1 mA	<0.02% + 0.5 mA	–	
Output Drift									
Voltage	Less than 0.1% + 5 mV total drift for 8 hours after an initial warm-up of 30 minutes.								
Current	Less than 0.1% + 10 mA total drift for 8 hours after an initial warm-up of 30 minutes.								
Temperature Range									
	0 to 40°C for full rated output. Derate output current 1% per °C between 40°C and 55°C							Derate output current 3.3% per °C	
Cooling	Convection cooling								
Isolation	±240 Vdc								
AC Input	100 Vac ±10%, 47– 63 Hz (opt. 0E9) 115 Vac ±10%, 47– 63 Hz (std) 230 Vac ±10%, 47– 63 Hz (opt. 0E3)								
Weight	3.8 kg (8.4 lb.) net, 5.1 kg (11.3 lbs) shipping			5.5 kg (12.1 lb.) net, 6.75 kg (14.9 lbs) shipping					Same as E3610A
Size	91 mm H x 213 mm W x 319 mm D 3.6" H x 8.4" W x 12.6" D			91 mm H x 213 mm W x 373 mm D 3.6" H x 8.4" W x 14.7" D					
Warranty	1 year								
Product Regulation	Certified to CSA 22.2 No. 231; conforms to IEC 1010-1; carries CE mark; complies with CISPR-11, Group 1, Class A								

Instek GPR-H D.C. Power Supply

D.C. POWER SUPPLY (200 ~ 500VA) GPR-H SERIES

SPECIFICATIONS

CONSTANT VOLTAGE OPERATION

Regulation	Line regulation ≤ 0.01% + 3mV
	Load regulation ≤ 0.01% + 5mV (< 10A)
	≤ 0.02% + 5mV (≥ 10A)
Ripple & Noise	≤ 1mVrms 5Hz ~ 1MHz
Recovery Time	≤ 100μS (50% Load change, Minimum load 0.5A)
Output Range	0 to rating voltage continuously adjustable

CONSTANT CURRENT OPERATION

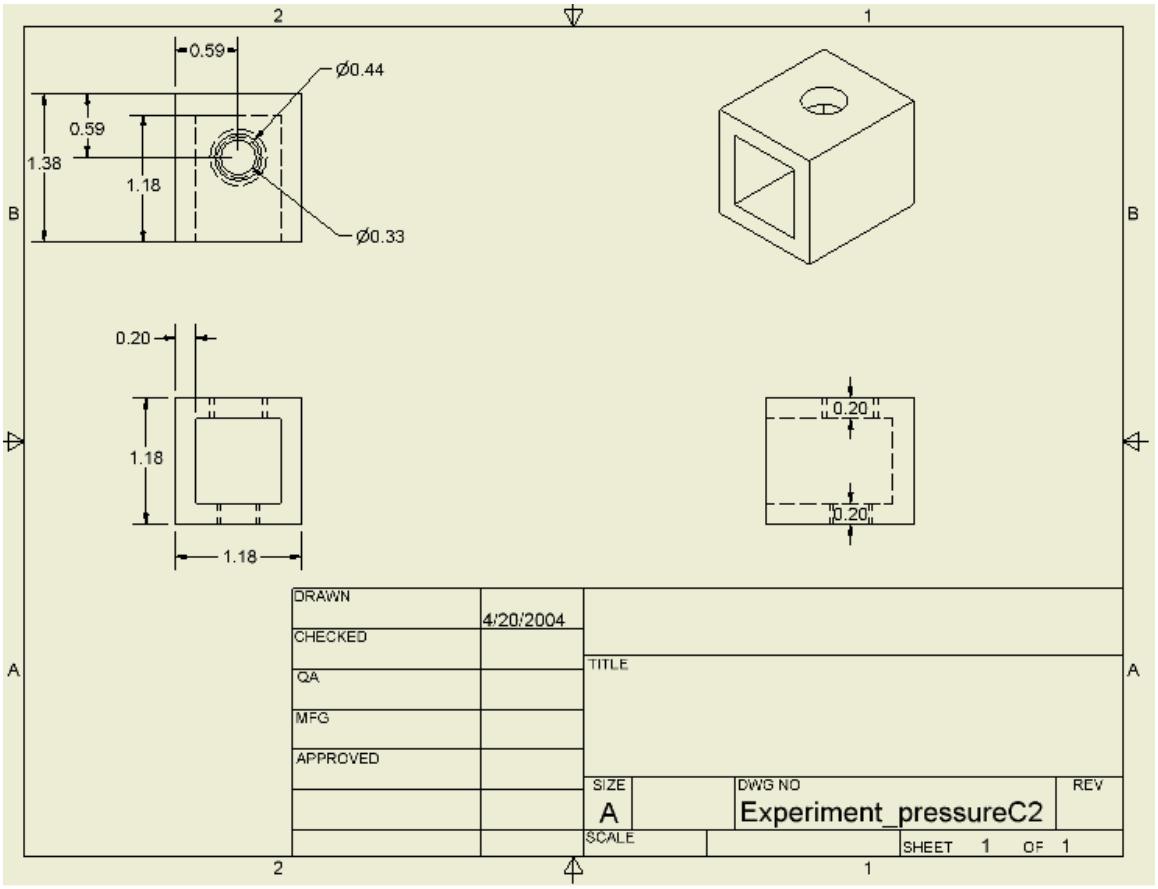
Regulation	Line regulation ≤ 0.2% + 3mA
	Load regulation ≤ 0.2% + 3mA
Ripple Current	≤ 5mArms(≤20A), ≤ 20mArms(≤50A)
Output Range	0 to rating amperes continuously adjustable

METER

Digital	3 1/2 digits 0.5" LED display
	Accuracy ± (0.5% of rdg + 2 digits)

- 0.01% High Regulation
- Constant Voltage and Constant Current Operation
- Internal Select for Continuous or Dynamic Load
- Low Ripple and Noise
- Overload and Reverse Polarity Protection
- 3 1/2 Digits 0.5" LED Display

Pressure Chamber



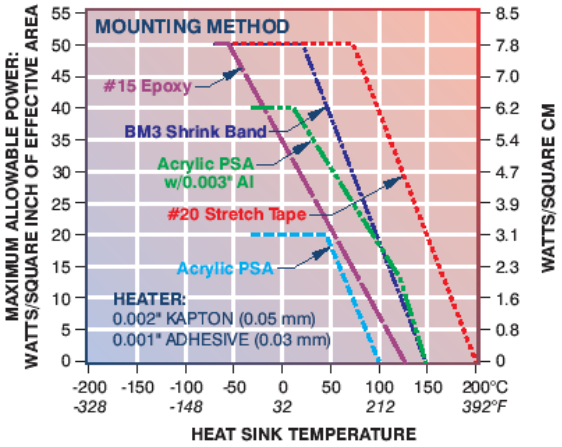
Minco Resistive Heaters

Specifications for catalog models

Temperature range: -200 to 200°C (-328 to 392°F). Upper lim with 0.003" (0.08 mm) foil backing is 150°C (302°F).
Material: Kapton/FEP, 0.002"/0.001" (0.05/0.03 mm).
Resistance tolerance: ±10% or ±0.5 Ω, whichever is greater
Dielectric strength: 1000 VRMS.
Minimum bend radius: 0.030" (0.8 mm).
Leadwire: Red PTFE insulated, stranded.
Current capacity (based on 100°C max. ambient temp.):

AWG 30	AWG 26	AWG 24	AWG 20
3.0 A	5.0 A	7.5 A	13.5 A

Maximum watt density, Kapton™ heaters



Example: At 50°C, the maximum power for a heater mounted with acrylic PSA is 18 W/in².

Size (inches) X	Size (inches) Y	Size (mm) X	Size (mm) Y	Type	Resistance in ohms*	Typical power	Effective area (in²)	Lead AWG	Model number
0.50	2.00	12.7	50.8	1 = ■	157	5 W at 28 V	0.79	30	HK5160R157L12

Agilent Data Acquisition Switch Unit

■ DC, Resistance, and Temperature Accuracy Specifications

± (% of reading + % of range) [1]
Includes measurement error, switching error, and transducer conversion error

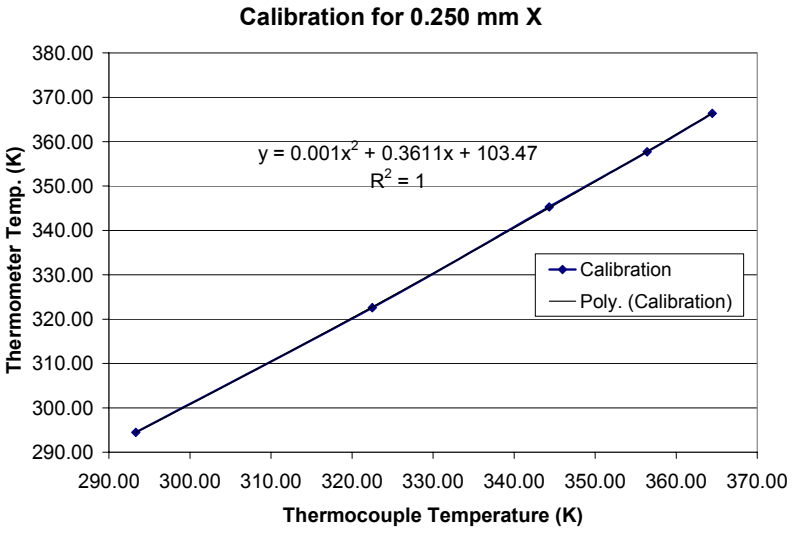
Function	Range [3]	Test Current or Burden Voltage	24 Hour [2] 23 °C ± 1 °C	90 Day 23 °C ± 5 °C	1 Year 23 °C ± 5 °C	Temperature Coefficient /°C 0 °C – 18 °C 28 °C – 55 °C
DC Voltage	100.0000 mV		0.0030 + 0.0035	0.0040 + 0.0040	0.0050 + 0.0040	0.0005 + 0.0005
	1.000000 V		0.0020 + 0.0006	0.0030 + 0.0007	0.0040 + 0.0007	0.0005 + 0.0001
	10.00000 V		0.0015 + 0.0004	0.0020 + 0.0005	0.0035 + 0.0005	0.0005 + 0.0001
	100.0000 V		0.0020 + 0.0006	0.0035 + 0.0006	0.0045 + 0.0006	0.0005 + 0.0001
	300.000 V		0.0020 + 0.0020	0.0035 + 0.0030	0.0045 + 0.0030	0.0005 + 0.0003
Resistance [4]	100.0000 Ω	1 mA current source	0.0030 + 0.0035	0.008 + 0.004	0.010 + 0.004	0.0006 + 0.0005
	1.000000 kΩ	1 mA	0.0020 + 0.0006	0.008 + 0.001	0.010 + 0.001	0.0006 + 0.0001
	10.00000 kΩ	100 µA	0.0020 + 0.0005	0.008 + 0.001	0.010 + 0.001	0.0006 + 0.0001
	100.0000 kΩ	10 µA	0.0020 + 0.0005	0.008 + 0.001	0.010 + 0.001	0.0006 + 0.0001
	1.000000 MΩ	5 µA	0.002 + 0.001	0.008 + 0.001	0.010 + 0.001	0.0010 + 0.0002
	10.00000 MΩ	500 nA	0.015 + 0.001	0.020 + 0.001	0.040 + 0.001	0.0030 + 0.0004
	100.0000 MΩ	500 nA || 10 MΩ	0.300 + 0.010	0.800 + 0.010	0.800 + 0.010	0.1500 + 0.0002
DC Current *34901A Only*	10.00000 mA	< 0.1 V burden	0.005 + 0.010	0.030 + 0.020	0.050 + 0.020	0.002 + 0.0020
	100.0000 mA	< 0.6 V	0.010 + 0.004	0.030 + 0.005	0.050 + 0.005	0.002 + 0.0005
	1.000000 A	< 2 V	0.050 + 0.006	0.080 + 0.010	0.100 + 0.010	0.005 + 0.0010
Temperature	**Type**	**Best Range Accuracy [5]**		**Extended Range Accuracy [5]**		
Thermocouple [6]	B	1100°C to 1820°C	1.2°C	400°C to 1100°C	1.8°C	0.03°C
	E	-150°C to 1000°C	1.0°C	-200°C to -150°C	1.5°C	0.03°C
	J	**-150°C to 1200°C**	**1.0°C**	**-210°C to -150°C**	**1.2°C**	**0.03°C**
	K	-100°C to 1200°C	1.0°C	-200°C to -100°C	1.5°C	0.03°C
	N	-100°C to 1300°C	1.0°C	-200°C to -100°C	1.5°C	0.03°C
	R	300°C to 1760°C	1.2°C	-50°C to 300°C	1.8°C	0.03°C
	S	400°C to 1760°C	1.2°C	-50°C to 400°C	1.8°C	0.03°C
	T	-100°C to 400°C	1.0°C	-200°C to -100°C	1.5°C	0.03°C
RTD	R_0 from 49Ω to 2.1 kΩ	-200°C to 600°C	0.06°C			0.003°C
Thermistor	2.2 k, 5 k, 10 k	-80°C to 150°C	0.08°C			0.002°C

[1] Specifications are for 1 hour warm up and 6½ digits
[2] Relative to calibration standards
[3] 20% over range on all ranges except 300 Vdc and 1 Adc ranges
[4] Specifications are for 4-wire ohms function or 2-wire ohms using Scaling to remove the offset. Without Scaling, add 4Ω additional error in 2-wire ohms function.
[5] 1 year accuracy. For total measurement accuracy, add temperature probe error.
[6] Thermocouple specifications not guaranteed when 34907A module is present

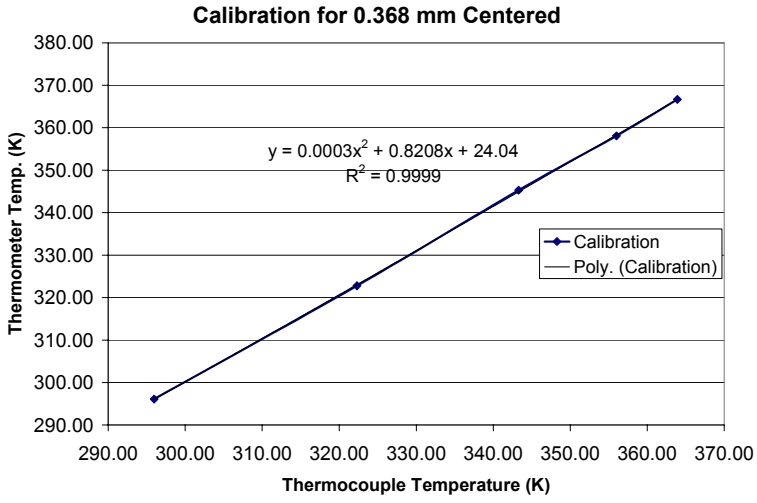
APPENDIX D

THERMOCOUPLE CALIBRATION CURVES

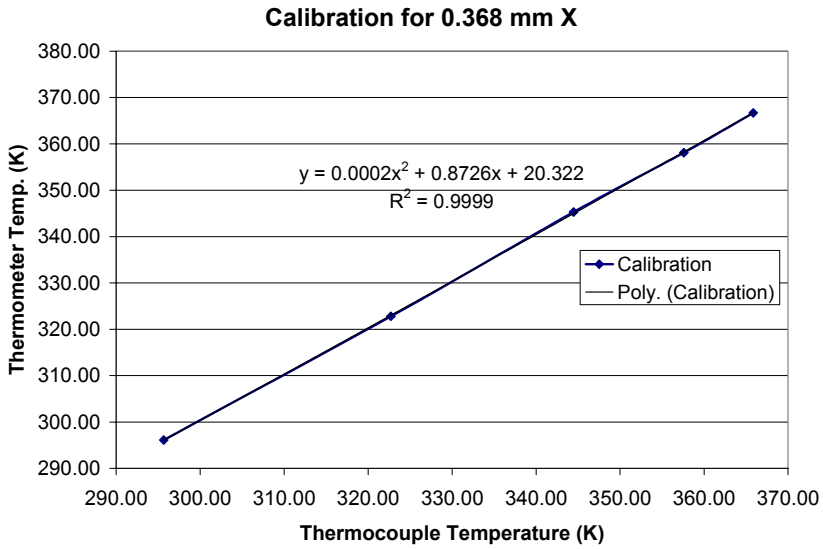
0.250 mm X Pattern Jet Holes



0.368 mm Centered Pattern Jet Holes



0.368 mm X Pattern Jet Holes



APPENDIX E

UNCERTAINTY ANALYSIS

There are two types of uncertainties in any type of experimentation. The first being fixed errors which are inherent in the instruments themselves and the second type are random errors. Random errors basically cover a broad scope of areas and can be accounted for in a probability analysis. Fixed errors are specified by the instrument manufacture or may result during calibration and can be quantified to represent a range in which the measurements are accurate. In the case of these experiments the fixed uncertainties occurred in the pressure transducer, flow meter, thermocouples, power supplies, and the data acquisition unit. These uncertainties were estimated so that the measurements of each instrument were as accurate as possible [Holman, 2001].

The random errors were seen in the data collected by the instruments. The factors that contributed to the random error were the room temperature variation, the initial temperature of each experiment, and the manual switching on and off of the heating and thermal management devices. There are many more random errors, but the ones mentioned account for the majority of discrepancies in the measurements, other than the fixed errors.

The room temperature varied between experiments ranging from 294 K to 298 K, which affected the temperature measurements. Probably one of the largest random errors

was the manual switching on and off of the power to the heater and thermal management systems. Every effort was taken to ensure as accurate starting time for the power to the heater and thermal management devices, however the time between each experiment varied by a 1-2 seconds. This extra variation contributed to the temperature profile over time which was evident in some of the graphs below.

The range of K-type thermocouples is 73 K- 1525 K, but has different accuracy at certain temperature ranges. Thermocouples can be classified into to categories. The first category is standard K-type thermocouple which has an accuracy of ± 2.2 K or 0.75% of full scale for the range of these experiments. The other category is called special limits K-type thermocouple that have an accuracy of ± 1.1 K or 0.4 % of full scale. The thermocouples embedded in the solder balls and PBGA package were special limit K-type thermocouples, however the extension wire used to connect the thermocouples to the data acquisition unit were standard K-type thermocouple wires. Also, the Agilent data acquisition unit adds ± 1 K of uncertainty to the temperature measurement making it a total of ± 2.1 K. Thus a temperature reading of 374 ± 2.1 K is accurate within the range of 371.9 K to 376.1 K.

An Agilent power supply provided power to the heater in the PBGA package and the solder balls. Another Agilent power supply delivered power to the pressure transducer and flow meter. The Instek power supply provided power to the compressors. The crucial uncertainty was with the power supply providing power to the PBGA heater and solder balls because it was used in validating the model. The Agilent E3620A power supply has two 3 ½ digital display which displays the voltage and current with an accuracy of 0.5% of the reading plus 2 counts. Plus two counts are added to both the

voltage and current as part of the uncertainty of the instrument. The power supplied to the heater and solder balls was calculated using

$$Q = V \cdot I \tag{E.1}$$

where V is the voltage and I current. Since the power supplied to the heater and solder balls was the important measurement the error was calculated based on the product function of error given by

$$w_Q = \left[\left(\left(\frac{\partial Q}{\partial V} + 2 \right) \cdot w_V \right)^2 + \left(\left(\frac{\partial Q}{\partial I} + 2 \right) \cdot w_I \right)^2 \right]^{1/2} \tag{E.2}$$

where $\frac{\partial Q}{\partial V}$ was the derivative of equation E.I with respect to voltage, $\frac{\partial Q}{\partial I}$ was the derivative of equation E.I with respect to current, w_V was the error in the voltage, and w_I was the error in the current. The + 2, which has the units of voltage and current, represents the plus two counts specified in the error. This equation was used to calculate the error in each reading. The recorded readings and error for voltage, current, and power for each experiment can be found at the end of Appendix E.

The error in the flow meter measurements can be calculated using the error product function as well. The flow meter outputs a linear signal ranging from 0-5 V based on the pressure in the chamber beneath the PCB. The uncertainty of the flow meter is ± 1 % of full scale. The data acquisition unit used a 5 ½ digital multi-meter to record this signal. Both the data acquisition unit and flow meter have error. The equation used to calculate the flow rate in liters per minute was

$$FR = \frac{FR_{\max}}{V_{\max}} \cdot V_{reading} \tag{E.3}$$

where $V_{reading}$ was the voltage output from the flow meter, $FR_{\max}$ was the maximum flow rate in liters per minute, and $V_{\max}$ was the maximum output voltage. The flow rate was an important factor in the validating the model.

The equation for error of the output voltage in the multi-meter of the data acquisition unit was found based on

$$w_{reading} = (0.00001) \cdot V_{\max} + (0.000047) \cdot V_{reading} + (0.000047) \cdot V_{\max} \tag{E.4}$$

where $V_{reading}$ was the voltage output from the flow meter and $V_{\max}$ was the maximum output voltage. Equation E.4 was then placed into

$$w_{FR} = \left[\left(\frac{\partial FR}{\partial FR_{\max}} \cdot w_{FR_{\max}} \right)^2 + \left(\frac{\partial FR}{\partial V_{\max}} \cdot w_{V_{\max}} \right)^2 + \left(\frac{\partial FR}{\partial V_{reading}} \cdot w_{V_{readingx}} \right)^2 \right]^{1/2} \tag{E.5}$$

where $\frac{\partial FR}{\partial FR_{\max}}$ was the derivative of equation E.3 with respect to the maximum flow rate, $\frac{\partial FR}{\partial V_{\max}}$ was the derivative of equation E.3 with respect to the maximum voltage output, and $\frac{\partial FR}{\partial V_{reading}}$ was the derivative of equation E.3 with respect to the voltage reading. The $w_{FR_{\max}}$, $w_{V_{\max}}$, and $w_{V_{reading}}$ were the uncertainties of maximum flow rate, the maximum voltage output, and voltage reading. Equation E.5 gives an uncertainty value to each flow rate measurement. The higher the flow rate, the greater the uncertainty. For example a flow rate of $1.64 \times 10^{-7} \pm 1.96 \times 10^{-8}$ m^3/s has a smaller error then a flow rate of $7.79 \times 10^{-7} \pm 2.56 \times 10^{-8}$ m^3/s. The average uncertainty for the flow range in which most of the experiments ran was $\pm 2.56 \times 10^{-8}$ m^3/s for the diaphragm compressor at

maximum capacity. The flow rate for the rotary compressor was much greater so the average uncertainty increased to ± 3.06 x 10^{-7} m^3/s at maximum capacity.

The pressure transducer uncertainty was computed in a similar method to the flow rate. The transducer outputted a 4-20 mAmp signal which represented a pressure range of 0-34.0 kPa gauge with an uncertainty of ± 0.25% of full scale. The linear equation used to convert the current signal to psi was

$$PR = \frac{PR_{\max}}{I_{range}} \cdot I_{reading} - 1.25 \qquad \text{(E.6)}$$

where $PR_{\max}$ was the maximum gauge pressure, I_{range} was the current output range, and $I_{reading}$ was the current output. The proper derivatives of the above formula where calculated and placed into an equation almost identical to equation E.5. The resulting average pressure uncertainty for the diaphragm compressor at maximum capacity was ± 100 Pa and for the rotary compressor at maximum capacity was ± 1.9 kPa. The uncertainty significantly changes as a function of the pressure transducer reading.

Repeatability in measurements was very important and can help explain some of the random errors that occur during experimentation. Each of the four sets of experiments had at least one repeat run. An experiment with identical parameters was run twice to check repeatability. The unbiased average standard deviation was then calculated to see how close the measurements were to each other based on an average between the two tests. The unbiased average standard deviation was calculated using

$$\sigma = \left[\frac{\sum_{i=1}^{n} (x_i - x_m)^2}{n-1} \right]^{1/2} \qquad \text{(E.7)}$$

where x_m was the average between the two measurements, x_i was the individual measurement, and n was the number of samples. The unbiased standard deviation was calculated for the flow meter, pressure measurements, and for temperature of one repeat test for each of the four sets of experiments.

Description and Power Settings for the Experiments

Experimental Procedures

	volts	amps	Power compressor (W)	Power Compressor Error (W) ±						
Hargraves BTC	12	0.18	2.16	0.0071		error = 0.5% of reading + 2 counts				
					Vary					
	Jet Diameters (mm)	**Hole Pattern**	**Minco Heater Current (amps)**	**Minco Heater Voltage**	**Minco Heating (W)**	**Minco Heating Error(W) ±**	**Solder ball Current (amps)**	**Solder Ball and Path Voltage**	**Solder ball joule heating (W)**	**Solder ball joule heating Error (W) ±**
	0.25	Center	0.308	3.28	1.010	0.0029	1.056	0.39	0.412	0.0019
	w/ only fan		0.306	3.31	1.013	0.0029	1.056	0.4	0.422	0.0019
			0.429	4.68	2.008	0.0036	1.057	0.42	0.444	0.0019
	w/ only fan		0.429	4.66	1.999	0.0035	1.056	0.4	0.422	0.0019
Repeat 1			0.522	5.76	3.007	0.0041	1.056	0.43	0.454	0.0020
	w/Fan		0.522	5.76	3.007	0.0041	1.056	0.43	0.454	0.0020
Repeat 1	w/ only fan		0.522	5.73	2.991	0.0041	1.027	0.43	0.442	0.0019
	w/Fan		0	0	0.000		1.68	0.6	1.008	0.0023
			0	0	0.000		1.68	0.6	1.008	0.0023
			0.428	4.67	1.999	0.0035	0	0	0.000	
		X	0.306	3.27	1.001	0.0029	1.057	0.42	0.444	0.0019
	w/ only fan		0.308	3.27	1.007	0.0029	1.056	0.4	0.422	0.0019
Repeat 1			0.431	4.64	2.000	0.0035	1.057	0.43	0.455	0.0020
Repeat 1	w/ only fan		0.434	4.62	2.005	0.0035	1.057	0.42	0.444	0.0019
			0.533	5.76	3.070	0.0041	1.056	0.44	0.465	0.0020
	w/Fan		0.529	5.76	3.047	0.0041	1.056	0.43	0.454	0.0020
	w/ only fan		0.529	5.68	3.005	0.0040	1.057	0.43	0.455	0.0020
	w/Fan		0	0	0.000		1.59	0.65	1.034	0.0022
			0	0	0.000		1.58	0.65	1.027	0.0022
			0.419	4.74	1.986	0.0036	0	0	0.000	
Repeat 1	0.3865	Center	0.31	3.25	1.008	0.0029	1.035	0.37	0.383	0.0019
Repeat 1	w/ only fan		0.31	3.25	1.008	0.0029	1.042	0.37	0.386	0.0019
			0.436	4.61	2.010	0.0035	1.043	0.38	0.396	0.0019
	w/ only fan		0.435	4.59	1.997	0.0035	1.057	0.4	0.423	0.0019
			0.531	5.65	3.000	0.0040	1.03	0.39	0.402	0.0019
	w/Fan		0.531	5.65	3.000	0.0040	1.03	0.39	0.402	0.0019
	w/ only fan		0.532	5.65	3.006	0.0040	1.047	0.4	0.419	0.0019
	w/Fan		0	0	0.000		1.67	0.6	1.002	0.0022
			0	0	0.000		1.67	0.6	1.002	0.0022
			0.432	4.61	1.992	0.0035	0	0	0.000	
		X	0.307	3.26	1.001	0.0029	0	0	0	
	w/ only fan		0.307	3.26	1.001	0.0029	0	0	0	
			0.43	4.61	1.982	0.0035	0	0	0	
	w/ only fan		0.43	4.61	1.982	0.0035	0	0	0	
Repeat 1			0.527	5.69	2.999	0.0040	0	0	0	
	w/Fan		0.527	5.69	2.999	0.0040	0	0	0	
	w/ only fan		0.527	5.69	2.999	0.0040	0	0	0	
	volts	amps	Power Compressor (W)	Power Compressor Error (W) ±						
Thomas Rotary	8.9	2	17.8	0.0058						
	Jet Diameters (mm)	**Hole Pattern**	**Minco Heater Current (amps)**	**Minco Heater Voltage**	**Minco Heating (W)**	**Minco Heating Error(W) ±**	**Solder ball Current (amps)**	**Solder Ball and Path Voltage**	**Solder ball joule heating (W)**	**Solder ball joule heating Error (W) ±**
	0.25	Center	0.523	5.76	3.012	0.0041	1.056	0.41	0.433	0.0019
	w/Fan		0.523	5.76	3.012	0.0041	1.056	0.41	0.433	0.0019
		X	0.529	5.76	3.047	0.0041	1.056	0.41	0.433	0.0019
	w/Fan		0.529	5.76	3.047	0.0041	1.056	0.41	0.433	0.0019
	0.368	Center	0.531	5.66	3.005	0.0040	1.057	0.38	0.402	0.0019
	w/Fan		0.531	5.66	3.005	0.0040	1.057	0.38	0.402	0.0019
		X	0.53	5.69	3.016	0.0040	1.02	0.39	0.398	0.0019
Repeat 1	w/Fan		0.522	5.69	2.970	0.0040	1.02	0.44	0.449	0.0019

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